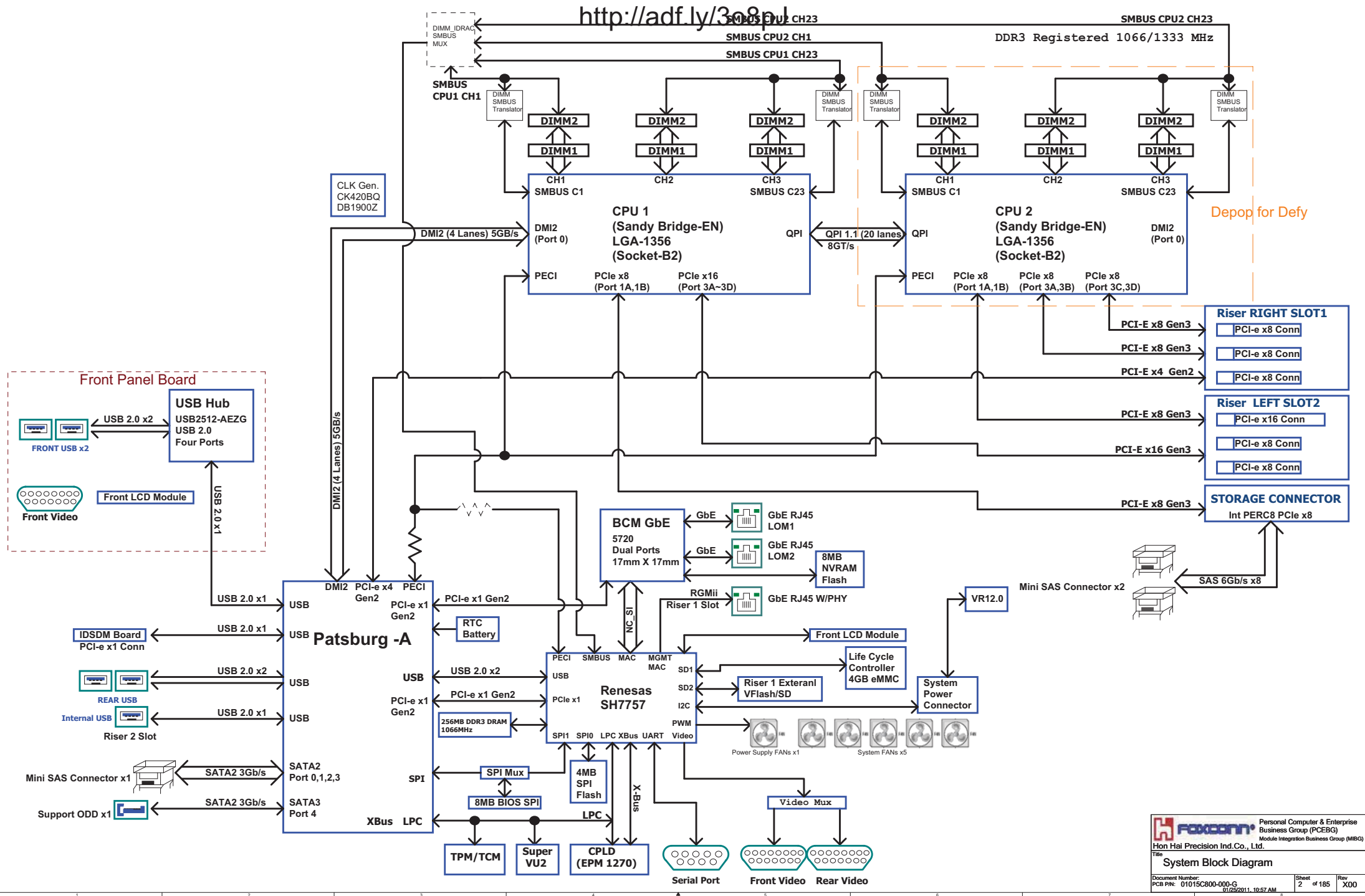


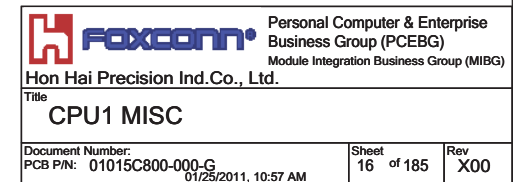
Revision	Description Of Changes	Date (M-D-Y)	Phase
X00	Preliminary release	01-24-2011	BU

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(47,48)	CPU1_M_CH1_DQ_63	AD3	DDR1_DQ<63>	DDR1_DQS_DP<17>	H30	CPU1_M_CH1_DQS_17_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_62	AD2	DDR1_DQ<62>	DDR1_DQS_DP<16>	AB3	CPU1_M_CH1_DQS_16_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_61	Y2	DDR1_DQ<61>	DDR1_DQS_DP<15>	AB9	CPU1_M_CH1_DQS_15_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_60	Y3	DDR1_DQ<60>	DDR1_DQS_DP<14>	R9	CPU1_M_CH1_DQS_14_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_59	AE2	DDR1_DQ<59>	DDR1_DQS_DP<13>	K8	CPU1_M_CH1_DQS_13_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_58	AE1	DDR1_DQ<58>	DDR1_DQS_DP<12>	L30	CPU1_M_CH1_DQS_12_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_57	AA3	DDR1_DQ<57>	DDR1_DQS_DP<11>	L34	CPU1_M_CH1_DQS_11_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_56	Y1	DDR1_DQ<56>	DDR1_DQS_DP<10>	R35	CPU1_M_CH1_DQS_10_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_55	AD8	DDR1_DQ<55>	DDR1_DQS_DP<9>	AB34	CPU1_M_CH1_DQS_09_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_54	AD9	DDR1_DQ<54>	DDR1_DQS_DP<8>	G29	CPU1_M_CH1_DQS_08_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_53	Y8	DDR1_DQ<53>	DDR1_DQS_DP<7>	AC1	CPU1_M_CH1_DQS_07_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_52	Y9	DDR1_DQ<52>	DDR1_DQS_DP<6>	AC8	CPU1_M_CH1_DQS_06_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_51	AE8	DDR1_DQ<51>	DDR1_DQS_DP<5>	T8	CPU1_M_CH1_DQS_05_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_50	AE9	DDR1_DQ<50>	DDR1_DQS_DP<4>	L7	CPU1_M_CH1_DQS_04_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_49	AA8	DDR1_DQ<49>	DDR1_DQS_DP<3>	K29	CPU1_M_CH1_DQS_03_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_48	AA9	DDR1_DQ<48>	DDR1_DQS_DP<2>	H34	CPU1_M_CH1_DQS_02_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_47	U8	DDR1_DQ<47>	DDR1_DQS_DP<1>	P36	CPU1_M_CH1_DQS_01_DP	(47,48)		
(47,48)	CPU1_M_CH1_DQ_46	U9	DDR1_DQ<46>	DDR1_DQS_DP<0>	AA36	CPU1_M_CH1_DQS_00_DP	(47,48)		
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(47,48)	CPU1_M_CH1_DQ_43	V8	DDR1_DQ<43>	DDR1_DQS_DN<16>	AC3	CPU1_M_CH1_DQS_16_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_42	V9	DDR1_DQ<42>	DDR1_DQS_DN<15>	AB8	CPU1_M_CH1_DQS_15_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_41	P8	DDR1_DQ<41>	DDR1_DQS_DN<14>	R8	CPU1_M_CH1_DQS_14_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_40	N8	DDR1_DQ<40>	DDR1_DQS_DN<13>	L8	CPU1_M_CH1_DQS_13_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_39	L6	DDR1_DQ<39>	DDR1_DQS_DN<12>	K30	CPU1_M_CH1_DQS_12_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_38	K6	DDR1_DQ<38>	DDR1_DQS_DN<11>	K34	CPU1_M_CH1_DQS_11_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_37	L10	DDR1_DQ<37>	DDR1_DQS_DN<10>	R36	CPU1_M_CH1_DQS_10_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_36	K10	DDR1_DQ<36>	DDR1_DQS_DN<9>	AB35	CPU1_M_CH1_DQS_09_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_35	L5	DDR1_DQ<35>	DDR1_DQS_DN<8>	H29	CPU1_M_CH1_DQS_08_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_34	K5	DDR1_DQ<34>	DDR1_DQS_DN<7>	AC2	CPU1_M_CH1_DQS_07_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_33	L9	DDR1_DQ<33>	DDR1_DQS_DN<6>	AC9	CPU1_M_CH1_DQS_06_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_32	K9	DDR1_DQ<32>	DDR1_DQS_DN<5>	T9	CPU1_M_CH1_DQS_05_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_31	K28	DDR1_DQ<31>	DDR1_DQS_DN<4>	K7	CPU1_M_CH1_DQS_04_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_30	L28	DDR1_DQ<30>	DDR1_DQS_DN<3>	L29	CPU1_M_CH1_DQS_03_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_29	K32	DDR1_DQ<29>	DDR1_DQS_DN<2>	H33	CPU1_M_CH1_DQS_02_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_28	L32	DDR1_DQ<28>	DDR1_DQS_DN<1>	P35	CPU1_M_CH1_DQS_01_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_27	K27	DDR1_DQ<27>	DDR1_DQS_DN<0>	AA35	CPU1_M_CH1_DQS_00_DN	(47,48)		
(47,48)	CPU1_M_CH1_DQ_26	L27	DDR1_DQ<26>						
(47,48)	CPU1_M_CH1_DQ_25	K31	DDR1_DQ<25>	DDR1_MA<15>	K24	CPU1_M_CH1_MA_15	(47,48)		
(47,48)	CPU1_M_CH1_DQ_24	L31	DDR1_DQ<24>	DDR1_MA<14>	J22	CPU1_M_CH1_MA_14	(47,48)		
(47,48)	CPU1_M_CH1_DQ_23	J33	DDR1_DQ<23>	DDR1_MA<13>	L13	CPU1_M_CH1_MA_13	(47,48)		
(47,48)	CPU1_M_CH1_DQ_22	J34	DDR1_DQ<22>	DDR1_MA<12>	J20	CPU1_M_CH1_MA_12	(47,48)		
(47,48)	CPU1_M_CH1_DQ_21	L35	DDR1_DQ<21>	DDR1_MA<11>	M24	CPU1_M_CH1_MA_11	(47,48)		
(47,48)	CPU1_M_CH1_DQ_20	L36	DDR1_DQ<20>	DDR1_MA<10>	M18	CPU1_M_CH1_MA_10	(47,48)		
(47,48)	CPU1_M_CH1_DQ_19	L33	DDR1_DQ<19>	DDR1_MA<9>	L25	CPU1_M_CH1_MA_09	(47,48)		
(47,48)	CPU1_M_CH1_DQ_18	K33	DDR1_DQ<18>	DDR1_MA<8>	K23	CPU1_M_CH1_MA_08	(47,48)		
(47,48)	CPU1_M_CH1_DQ_17	K36	DDR1_DQ<17>	DDR1_MA<7>	L23	CPU1_M_CH1_MA_07	(47,48)		
(47,48)	CPU1_M_CH1_DQ_16	K35	DDR1_DQ<16>	DDR1_MA<6>	L22	CPU1_M_CH1_MA_06	(47,48)		
(47,48)	CPU1_M_CH1_DQ_15	N34	DDR1_DQ<15>	DDR1_MA<5>	K22	CPU1_M_CH1_MA_05	(47,48)		
(47,48)	CPU1_M_CH1_DQ_14	P34	DDR1_DQ<14>	DDR1_MA<4>	M22	CPU1_M_CH1_MA_04	(47,48)		
(47,48)	CPU1_M_CH1_DQ_13	U36	DDR1_DQ<13>	DDR1_MA<3>	L21	CPU1_M_CH1_MA_03	(47,48)		
(47,48)	CPU1_M_CH1_DQ_12	U35	DDR1_DQ<12>	DDR1_MA<2>	K20	CPU1_M_CH1_MA_02	(47,48)		
(47,48)	CPU1_M_CH1_DQ_11	N35	DDR1_DQ<11>	DDR1_MA<1>	L20	CPU1_M_CH1_MA_01	(47,48)		
(47,48)	CPU1_M_CH1_DQ_10	N36	DDR1_DQ<10>	DDR1_MA<0>	K19	CPU1_M_CH1_MA_00	(47,48)		
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(47,48)	CPU1_M_CH1_DQ_08	T35	DDR1_DQ<8>	DDR1_ECC<7>	G28	CPU1_M_CH1_ECC_7	(47,48)		
(47,48)	CPU1_M_CH1_DQ_07	Y36	DDR1_DQ<7>	DDR1_ECC<6>	H28	CPU1_M_CH1_ECC_6	(47,48)		
(47,48)	CPU1_M_CH1_DQ_06	Y35	DDR1_DQ<6>	DDR1_ECC<5>	H32	CPU1_M_CH1_ECC_5	(47,48)		
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(47,48)	CPU1_M_CH1_DQ_04	AD34	DDR1_DQ<4>	DDR1_ECC<3>	G27	CPU1_M_CH1_ECC_3	(47,48)		
(47,48)	CPU1_M_CH1_DQ_03	W36	DDR1_DQ<3>	DDR1_ECC<2>	H27	CPU1_M_CH1_ECC_2	(47,48)		
(47,48)	CPU1_M_CH1_DQ_02	W35	DDR1_DQ<2>	DDR1_ECC<1>	G31	CPU1_M_CH1_ECC_1	(47,48)		
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(48)	CPU1_M_CH1_CS_6_N	L12	DDR1_CS_N<6>	DDR1_CKE<2>	J25	CPU1_M_CH1_CKE_2	(47,48)		
(48)	CPU1_M_CH1_CS_5_N	H14	DDR1_CS_N<5>	DDR1_CKE<1>	J26	CPU1_M_CH1_CKE_1	(47,48)		
(48)	CPU1_M_CH1_CS_4_N	K15	DDR1_CS_N<4>	DDR1_CKE<0>	K25	CPU1_M_CH1_CKE_0	(47,48)		
(47)	CPU1_M_CH1_CS_3_N	K12	DDR1_CS_N<3>						
(47)	CPU1_M_CH1_CS_2_N	L11	DDR1_CS_N<2>	DDR1_BA<2>	J24	CPU1_M_CH1_BA_2	(47,48)		
(47)	CPU1_M_CH1_CS_1_N	L15	DDR1_CS_N<1>	DDR1_BA<1>	L18	CPU1_M_CH1_BA_1	(47,48)		
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(47)	CPU1_M_CH1_CLK_2_DP	J16	DDR1_CLK_DP<2>	DDR1_ODT<3>	G13	CPU1_M_CH1_ODT_3	(47,48)		
(48)	CPU1_M_CH1_CLK_1_DP	H19	DDR1_CLK_DP<1>	DDR1_ODT<2>	J14	CPU1_M_CH1_ODT_2	(47,48)		
(47)	CPU1_M_CH1_CLK_0_DP	J17	DDR1_CLK_DP<0>	DDR1_ODT<1>	H13	CPU1_M_CH1_ODT_1	(47,48)		
				DDR1_ODT<0>	G15	CPU1_M_CH1_ODT_0	(47,48)		
(48)	CPU1_M_CH1_CLK_3_DN	H18	DDR1_CLK_DN<3>	DDR1_WE_N	K14	CPU1_M_CH1_WE_N	(47,48)		
(47)	CPU1_M_CH1_CLK_2_DN	H16	DDR1_CLK_DN<2>	DDR1_RAS_N	K17	CPU1_M_CH1_RAS_N	(47,48)		
(48)	CPU1_M_CH1_CLK_1_DN	G19	DDR1_CLK_DN<1>	DDR1_PAR_ERR_N	J21	CPU1_M_CH1_PERR_N	(47,48)		
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				DDR1_MA_PAR	J19	CPU1_M_CH1_MA_PAR	(47,48)		

CPU1C		
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(50,51) CPU1_M_CH2_DQ_40	G9	DDR2_DQ<40>
(50,51) CPU1_M_CH2_DQ_39	F6	DDR2_DQ<39>
(50,51) CPU1_M_CH2_DQ_38	D6	DDR2_DQ<38>
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DDR2_DQS_DP<15>	R6	CPU1_M_CH2_DQS_15_DP (50,51)
DDR2_DQS_DP<14>	G8	CPU1_M_CH2_DQS_14_DP (50,51)
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DDR2_DQS_DP<12>	H39	CPU1_M_CH2_DQS_12_DP (50,51)
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DDR2_DQS_DN<9>	AB38	CPU1_M_CH2_DQS_09_DN (50,51)
DDR2_DQS_DN<8>	E31	CPU1_M_CH2_DQS_08_DN (50,51)
DDR2_DQS_DN<7>	AC6	CPU1_M_CH2_DQS_07_DN (50,51)
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DDR2_DQS_DN<5>	G7	CPU1_M_CH2_DQS_05_DN (50,51)
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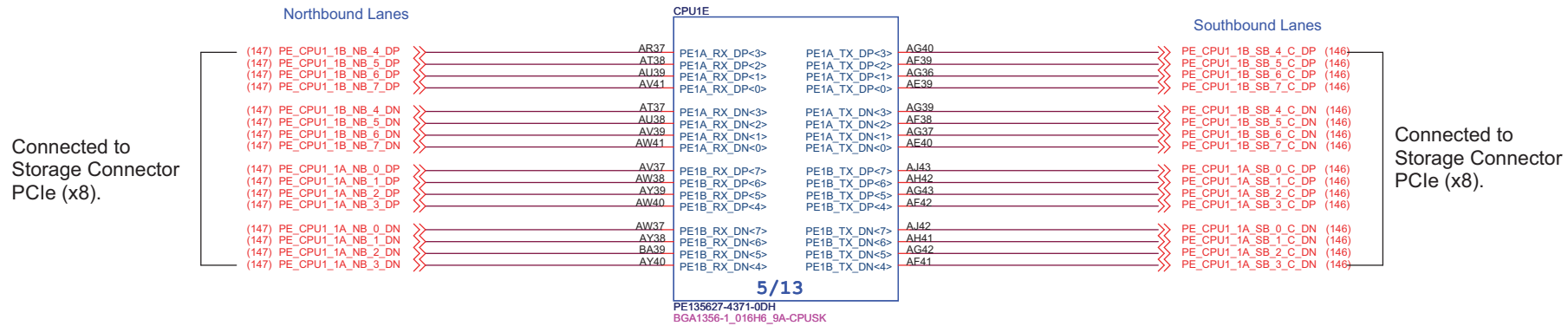
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DDR3_DQS_DP<6>	L2	CPU1_M_CH3_DQS_06_DP (53,54)
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DDR3_DQS_DP<3>	D42	CPU1_M_CH3_DQS_03_DP (53,54)
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DDR3_DQS_DP<1>	R42	CPU1_M_CH3_DQS_01_DP (53,54)
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DDR3_MA<13>	D14	CPU1_M_CH3_MA_13 (53,54)
DDR3_MA<12>	B26	CPU1_M_CH3_MA_12 (53,54)
DDR3_MA<11>	A25	CPU1_M_CH3_MA_11 (53,54)
DDR3_MA<10>	A17	CPU1_M_CH3_MA_10 (53,54)
DDR3_MA<9>	B25	CPU1_M_CH3_MA_09 (53,54)
DDR3_MA<8>	B24	CPU1_M_CH3_MA_08 (53,54)
DDR3_MA<7>	D25	CPU1_M_CH3_MA_07 (53,54)
DDR3_MA<6>	C23	CPU1_M_CH3_MA_06 (53,54)
DDR3_MA<5>	C24	CPU1_M_CH3_MA_05 (53,54)
DDR3_MA<4>	D23	CPU1_M_CH3_MA_04 (53,54)
DDR3_MA<3>	C22	CPU1_M_CH3_MA_03 (53,54)
DDR3_MA<2>	D22	CPU1_M_CH3_MA_02 (53,54)
DDR3_MA<1>	D21	CPU1_M_CH3_MA_01 (53,54)
DDR3_MA<0>	C17	CPU1_M_CH3_MA_00 (53,54)
DDR3_ECC<7>	A31	CPU1_M_CH3_ECC_7 (53,54)
DDR3_ECC<6>	B31	CPU1_M_CH3_ECC_6 (53,54)
DDR3_ECC<5>	B35	CPU1_M_CH3_ECC_5 (53,54)
DDR3_ECC<4>	C35	CPU1_M_CH3_ECC_4 (53,54)
DDR3_ECC<3>	A30	CPU1_M_CH3_ECC_3 (53,54)
DDR3_ECC<2>	B30	CPU1_M_CH3_ECC_2 (53,54)
DDR3_ECC<1>	C33	CPU1_M_CH3_ECC_1 (53,54)
DDR3_ECC<0>	C34	CPU1_M_CH3_ECC_0 (53,54)
DDR3_CKE<3>	C28	CPU1_M_CH3_CKE_3 (54)
DDR3_CKE<2>	A28	CPU1_M_CH3_CKE_2 (54)
DDR3_CKE<1>	B29	CPU1_M_CH3_CKE_1 (53)
DDR3_CKE<0>	B28	CPU1_M_CH3_CKE_0 (53)
DDR3_BA<2>	C27	CPU1_M_CH3_BA_2 (53,54)
DDR3_BA<1>	D17	CPU1_M_CH3_BA_1 (53,54)
DDR3_BA<0>	B16	CPU1_M_CH3_BA_0 (53,54)
DDR3_ODT<3>	C13	CPU1_M_CH3_ODT_3 (54)
DDR3_ODT<2>	C14	CPU1_M_CH3_ODT_2 (54)
DDR3_ODT<1>	C12	CPU1_M_CH3_ODT_1 (53)
DDR3_ODT<0>	D15	CPU1_M_CH3_ODT_0 (53)
DDR3_WE_N	C16	CPU1_M_CH3_WE_N (53,54)
DDR3_RAS_N	A16	CPU1_M_CH3_RAS_N (53,54)
DDR3_PAR_ERR_N	A26	CPU1_M_CH3_PERR_N (53,54)
DDR3_CAS_N	B15	CPU1_M_CH3_CAS_N (53,54)
DDR3_MA_PAR	C18	CPU1_M_CH3_MA_PAR (53,54)

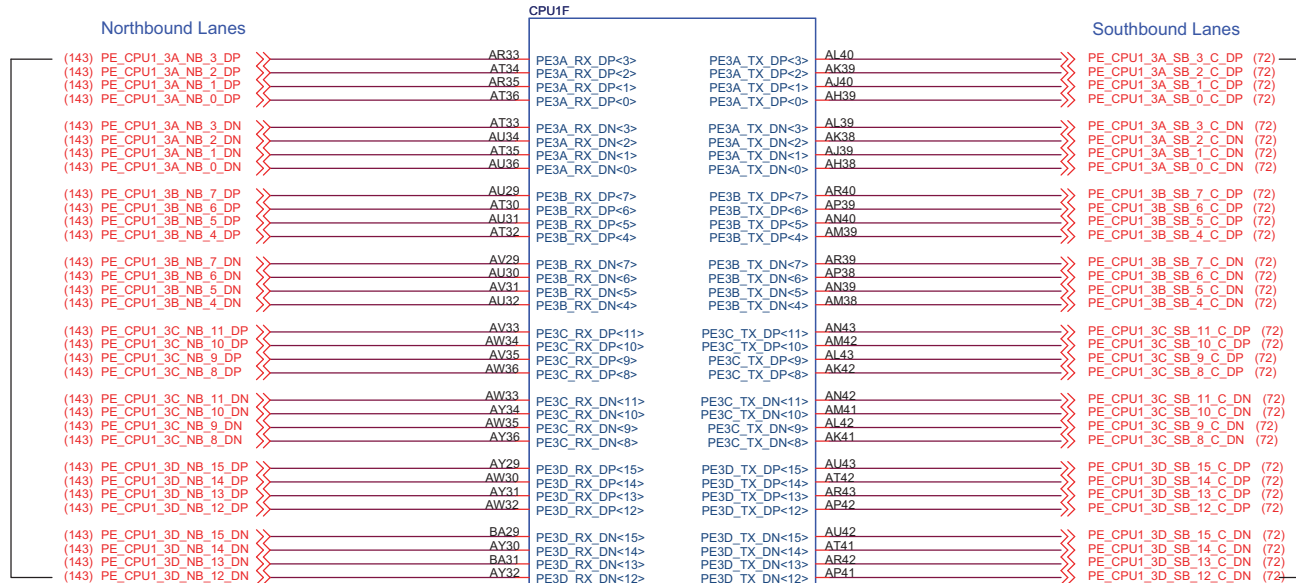
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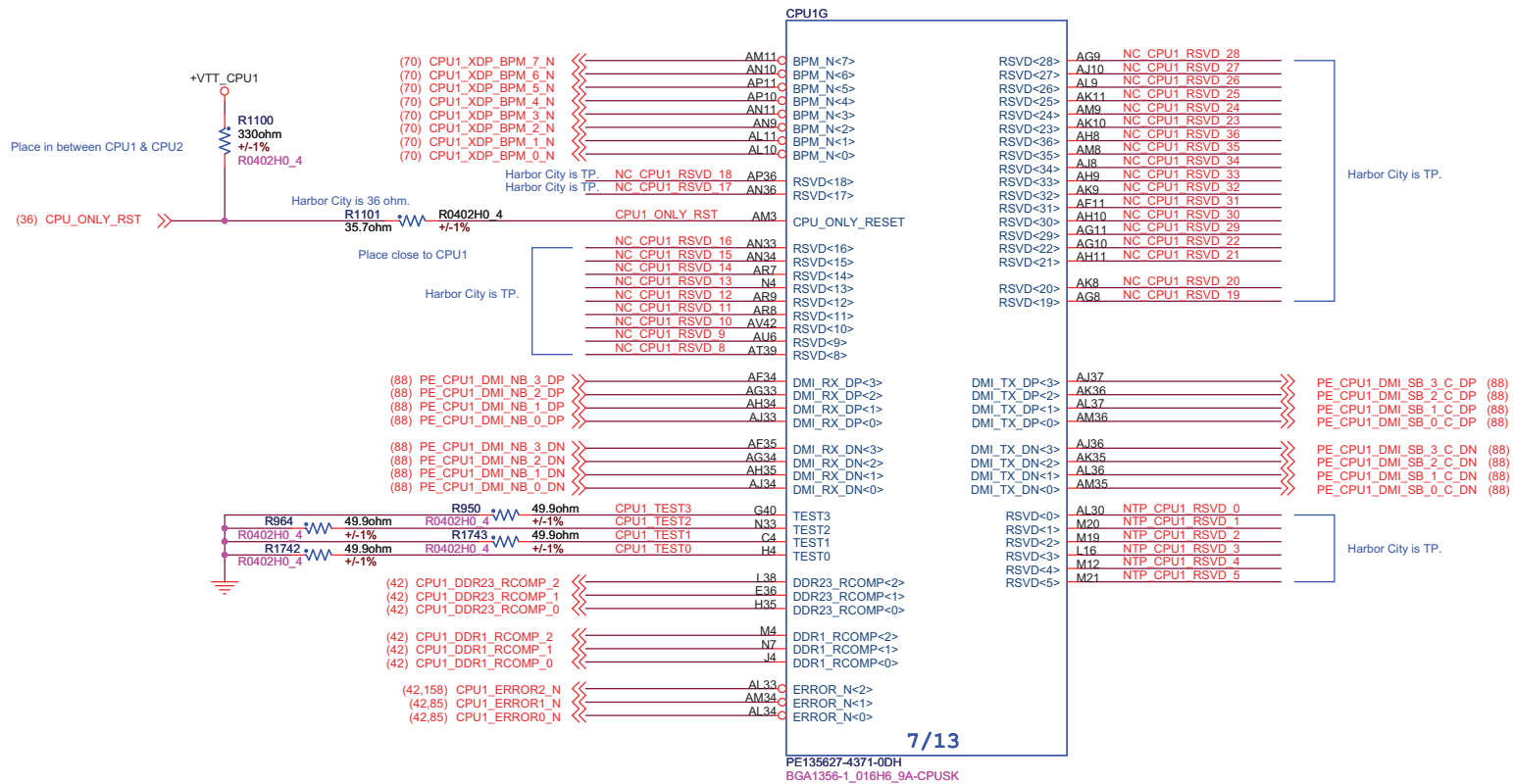
Connected to Riser 2 Slot
(Slot 2 ; 280 pin)

Connected to Riser 2 Slot
(Slot 2 ; 280 pin)

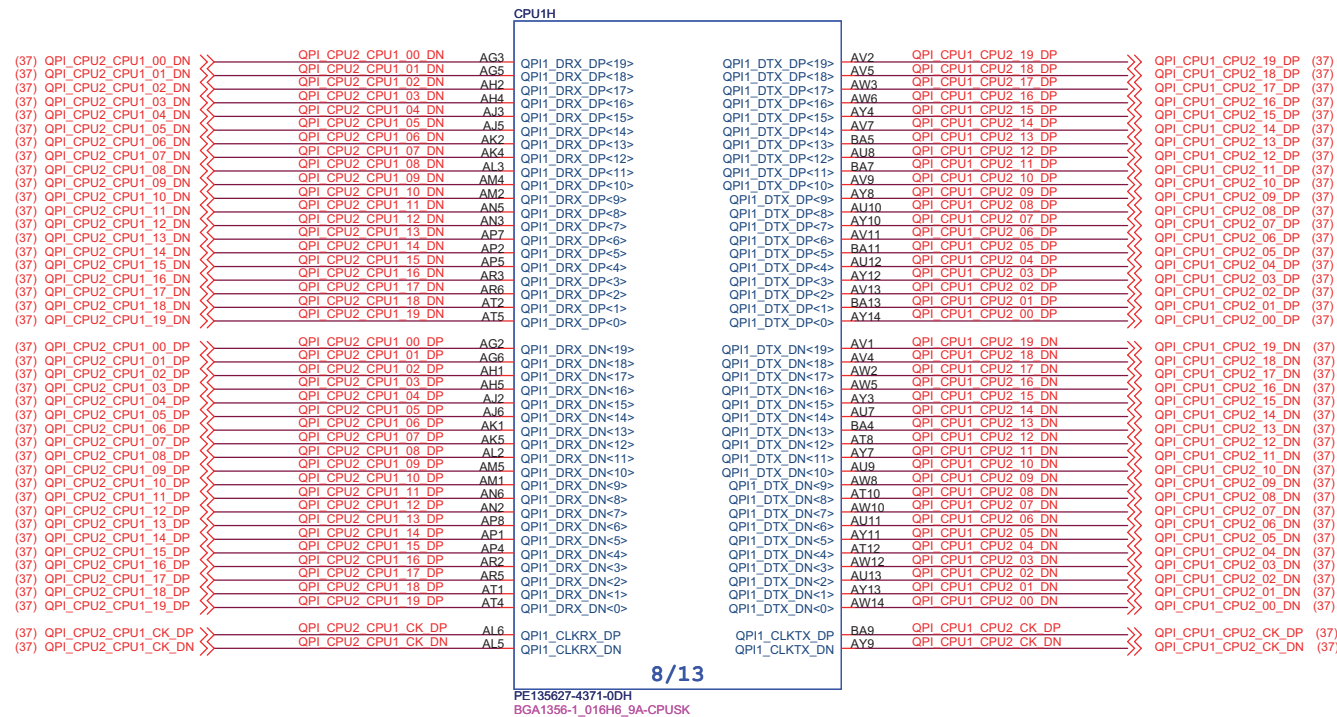


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Lane Reversed & DP\DN swapped on most lanes.(Reference Harbor City CRB Rev 1.0)
For routing need to redefine.

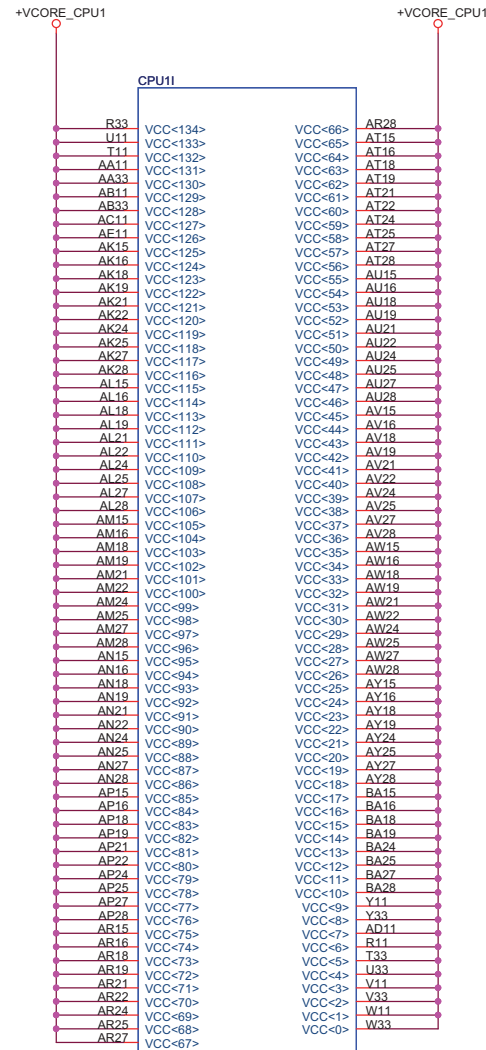


QPI LINK CONNECTIVITY (REFER TO HARBOR CITY CRB Rev1.0)

Name	CPU1 PIN NAME	CPU2 PIN NAME	LANE REVERSAL	POLARITY INVERSION
QPI_CPU1_CPU2_DP(19..0)	QPI1_DTX_DP(19..0)	QPI1_DRX_DN(0..19)	YES-ALL LANES	YES-ALL LANES
QPI_CPU1_CPU2_DN(19..0)	QPI1_DTX_DN(19..0)	QPI1_DRX_DP(0..19)	YES-ALL LANES	YES-ALL LANES
QPI_CPU2_CPU1_DP(19..0)	QPI1_DRX_DN(0..19)	QPI1_DTX_DP(19..0)	YES-ALL LANES	YES-ALL LANES
QPI_CPU2_CPU1_DN(19..0)	QPI1_DRX_DP(0..19)	QPI1_DTX_DN(19..0)	YES-ALL LANES	YES-ALL LANES

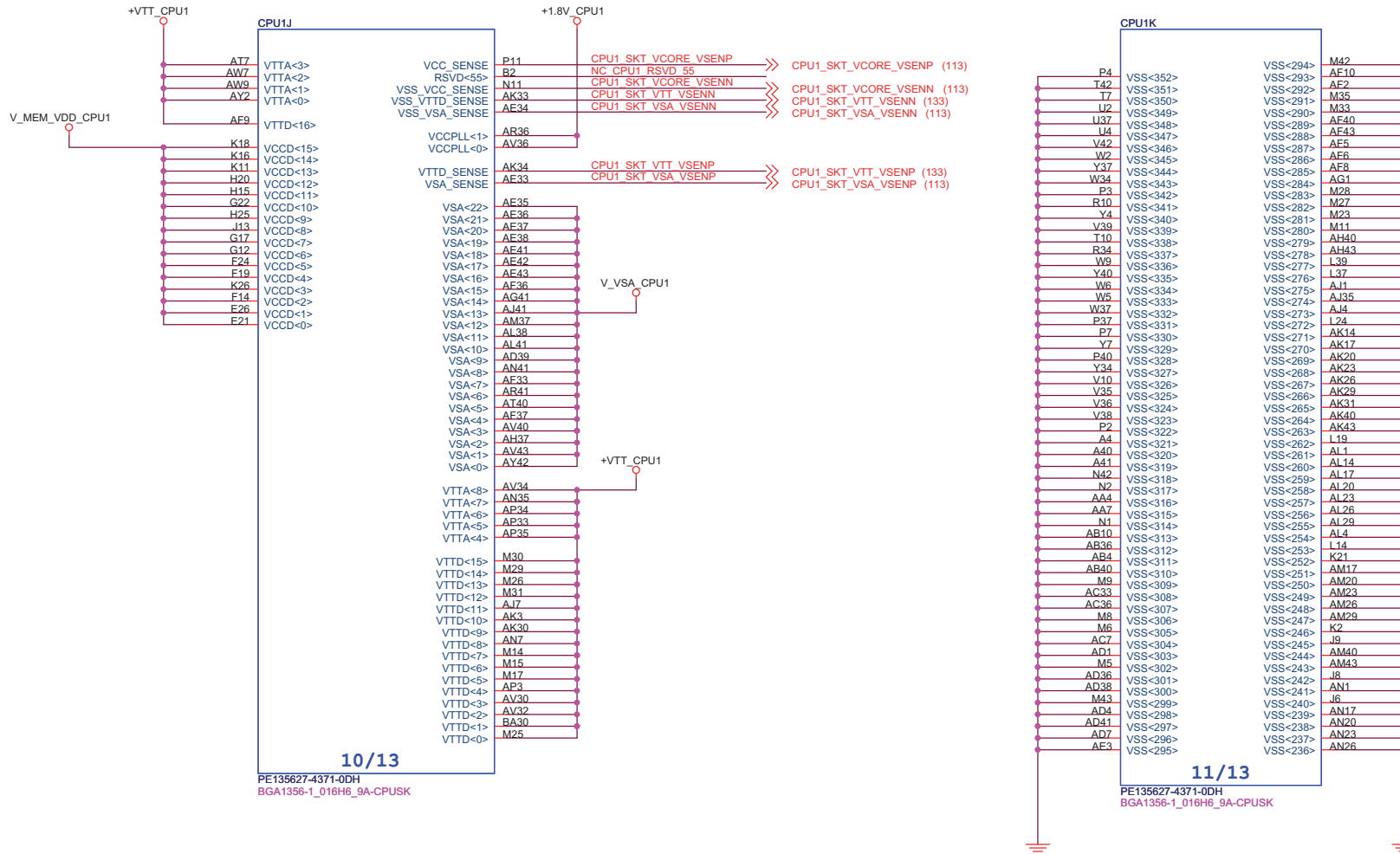
BUS NAMING CONVENTION : TECHNOLOGY_FROM_TO POLARITY

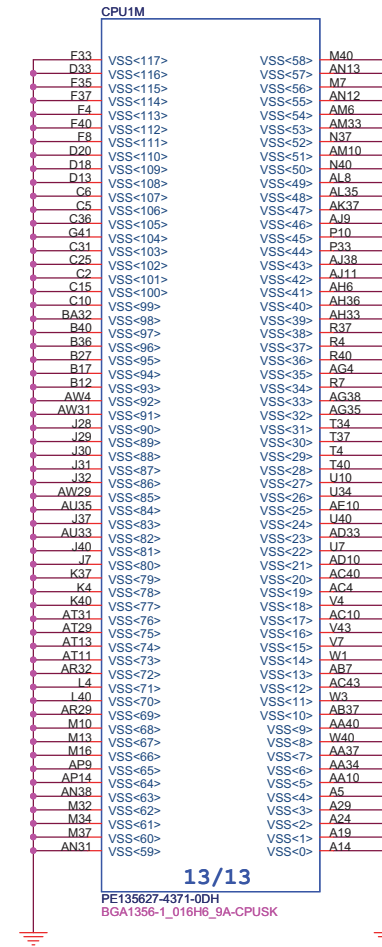
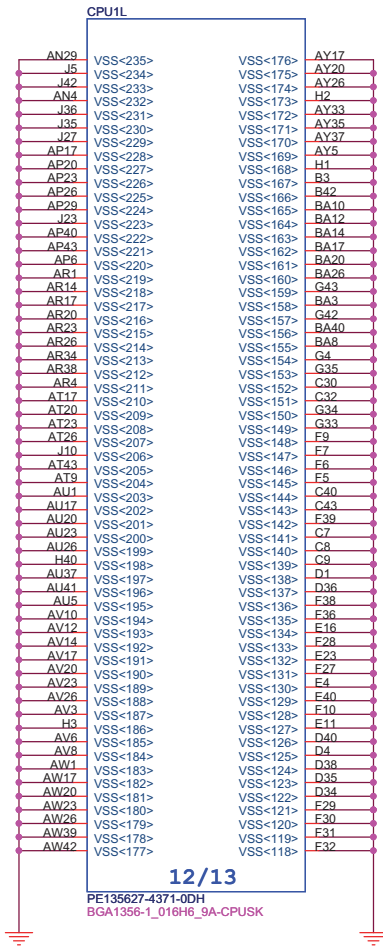
EXAMPLE : QPI_CPU1_CPU2_DP = QPI TECH, FROM CPU1, TO CPU2, DP POLARITY

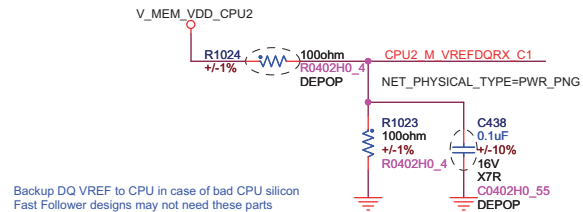
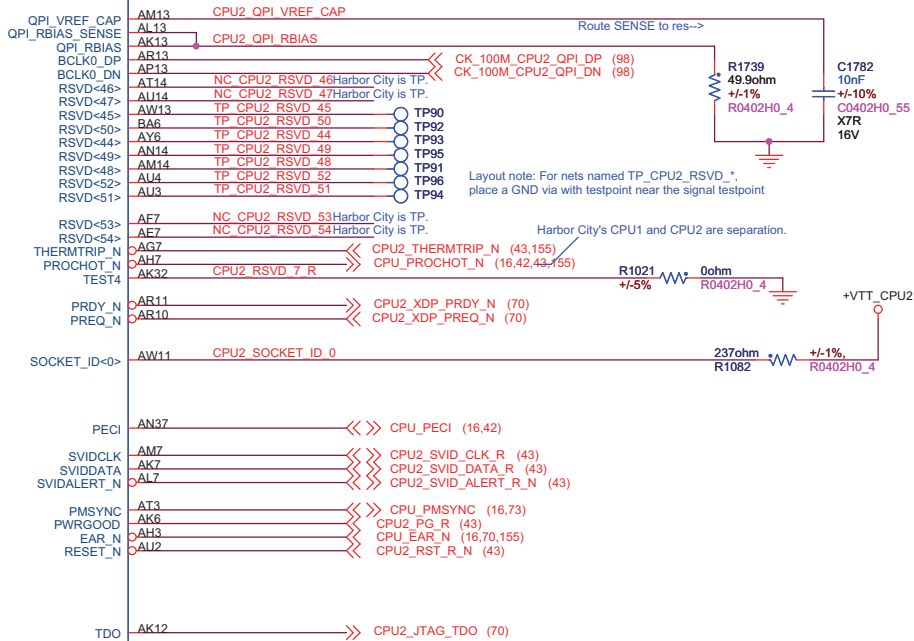


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CPU2B

(60.61) CPU2_M_CH1_DQ_63	AD3	DDR1_DQ<63>	H30	CPU2_M_CH1_DQS_17_DP (60.61)
(60.61) CPU2_M_CH1_DQ_62	AD2	DDR1_DQ<62>	AB3	CPU2_M_CH1_DQS_16_DP (60.61)
(60.61) CPU2_M_CH1_DQ_61	Y2	DDR1_DQ<61>	AB9	CPU2_M_CH1_DQS_15_DP (60.61)
(60.61) CPU2_M_CH1_DQ_60	Y3	DDR1_DQ<60>	R9	CPU2_M_CH1_DQS_14_DP (60.61)
(60.61) CPU2_M_CH1_DQ_59	AE2	DDR1_DQ<59>	K8	CPU2_M_CH1_DQS_13_DP (60.61)
(60.61) CPU2_M_CH1_DQ_58	AE1	DDR1_DQ<58>	L30	CPU2_M_CH1_DQS_12_DP (60.61)
(60.61) CPU2_M_CH1_DQ_57	AA3	DDR1_DQ<57>	L34	CPU2_M_CH1_DQS_11_DP (60.61)
(60.61) CPU2_M_CH1_DQ_56	Y1	DDR1_DQ<56>	R35	CPU2_M_CH1_DQS_10_DP (60.61)
(60.61) CPU2_M_CH1_DQ_55	AD8	DDR1_DQ<55>	AB34	CPU2_M_CH1_DQS_09_DP (60.61)
(60.61) CPU2_M_CH1_DQ_54	AD9	DDR1_DQ<54>	G29	CPU2_M_CH1_DQS_08_DP (60.61)
(60.61) CPU2_M_CH1_DQ_53	Y8	DDR1_DQ<53>	AC1	CPU2_M_CH1_DQS_07_DP (60.61)
(60.61) CPU2_M_CH1_DQ_52	Y9	DDR1_DQ<52>	AC8	CPU2_M_CH1_DQS_06_DP (60.61)
(60.61) CPU2_M_CH1_DQ_51	AE8	DDR1_DQ<51>	T8	CPU2_M_CH1_DQS_05_DP (60.61)
(60.61) CPU2_M_CH1_DQ_50	AE9	DDR1_DQ<50>	L7	CPU2_M_CH1_DQS_04_DP (60.61)
(60.61) CPU2_M_CH1_DQ_49	AA8	DDR1_DQ<49>	K29	CPU2_M_CH1_DQS_03_DP (60.61)
(60.61) CPU2_M_CH1_DQ_48	AA9	DDR1_DQ<48>	H34	CPU2_M_CH1_DQS_02_DP (60.61)
(60.61) CPU2_M_CH1_DQ_47	U8	DDR1_DQ<47>	P36	CPU2_M_CH1_DQS_01_DP (60.61)
(60.61) CPU2_M_CH1_DQ_46	U9	DDR1_DQ<46>	AA36	CPU2_M_CH1_DQS_00_DP (60.61)
(60.61) CPU2_M_CH1_DQ_45	P9	DDR1_DQ<45>		
(60.61) CPU2_M_CH1_DQ_44	N9	DDR1_DQ<44>	G30	CPU2_M_CH1_DQS_17_DN (60.61)
(60.61) CPU2_M_CH1_DQ_43	V8	DDR1_DQ<43>	AC3	CPU2_M_CH1_DQS_16_DN (60.61)
(60.61) CPU2_M_CH1_DQ_42	V9	DDR1_DQ<42>	AB8	CPU2_M_CH1_DQS_15_DN (60.61)
(60.61) CPU2_M_CH1_DQ_41	P8	DDR1_DQ<41>	R8	CPU2_M_CH1_DQS_14_DN (60.61)
(60.61) CPU2_M_CH1_DQ_40	N8	DDR1_DQ<40>	L8	CPU2_M_CH1_DQS_13_DN (60.61)
(60.61) CPU2_M_CH1_DQ_39	L6	DDR1_DQ<39>	K30	CPU2_M_CH1_DQS_12_DN (60.61)
(60.61) CPU2_M_CH1_DQ_38	K6	DDR1_DQ<38>	K34	CPU2_M_CH1_DQS_11_DN (60.61)
(60.61) CPU2_M_CH1_DQ_37	L10	DDR1_DQ<37>	R36	CPU2_M_CH1_DQS_10_DN (60.61)
(60.61) CPU2_M_CH1_DQ_36	K10	DDR1_DQ<36>	AB35	CPU2_M_CH1_DQS_09_DN (60.61)
(60.61) CPU2_M_CH1_DQ_35	L5	DDR1_DQ<35>	H29	CPU2_M_CH1_DQS_08_DN (60.61)
(60.61) CPU2_M_CH1_DQ_34	K5	DDR1_DQ<34>	AC2	CPU2_M_CH1_DQS_07_DN (60.61)
(60.61) CPU2_M_CH1_DQ_33	L9	DDR1_DQ<33>	AC9	CPU2_M_CH1_DQS_06_DN (60.61)
(60.61) CPU2_M_CH1_DQ_32	K9	DDR1_DQ<32>	T9	CPU2_M_CH1_DQS_05_DN (60.61)
(60.61) CPU2_M_CH1_DQ_31	K28	DDR1_DQ<31>	K7	CPU2_M_CH1_DQS_04_DN (60.61)
(60.61) CPU2_M_CH1_DQ_30	L28	DDR1_DQ<30>	L29	CPU2_M_CH1_DQS_03_DN (60.61)
(60.61) CPU2_M_CH1_DQ_29	K32	DDR1_DQ<29>	H33	CPU2_M_CH1_DQS_02_DN (60.61)
(60.61) CPU2_M_CH1_DQ_28	L32	DDR1_DQ<28>	P35	CPU2_M_CH1_DQS_01_DN (60.61)
(60.61) CPU2_M_CH1_DQ_27	K27	DDR1_DQ<27>	AA35	CPU2_M_CH1_DQS_00_DN (60.61)
(60.61) CPU2_M_CH1_DQ_26	L27	DDR1_DQ<26>		
(60.61) CPU2_M_CH1_DQ_25	K31	DDR1_DQ<25>	K24	CPU2_M_CH1_MA_15 (60.61)
(60.61) CPU2_M_CH1_DQ_24	L31	DDR1_DQ<24>	J22	CPU2_M_CH1_MA_14 (60.61)
(60.61) CPU2_M_CH1_DQ_23	J33	DDR1_DQ<23>	L13	CPU2_M_CH1_MA_13 (60.61)
(60.61) CPU2_M_CH1_DQ_22	J34	DDR1_DQ<22>	J20	CPU2_M_CH1_MA_12 (60.61)
(60.61) CPU2_M_CH1_DQ_21	L35	DDR1_DQ<21>	M24	CPU2_M_CH1_MA_11 (60.61)
(60.61) CPU2_M_CH1_DQ_20	L36	DDR1_DQ<20>	M18	CPU2_M_CH1_MA_10 (60.61)
(60.61) CPU2_M_CH1_DQ_19	L33	DDR1_DQ<19>	L25	CPU2_M_CH1_MA_09 (60.61)
(60.61) CPU2_M_CH1_DQ_18	K33	DDR1_DQ<18>	K23	CPU2_M_CH1_MA_08 (60.61)
(60.61) CPU2_M_CH1_DQ_17	K36	DDR1_DQ<17>	L23	CPU2_M_CH1_MA_07 (60.61)
(60.61) CPU2_M_CH1_DQ_16	K35	DDR1_DQ<16>	L22	CPU2_M_CH1_MA_06 (60.61)
(60.61) CPU2_M_CH1_DQ_15	N34	DDR1_DQ<15>	K22	CPU2_M_CH1_MA_05 (60.61)
(60.61) CPU2_M_CH1_DQ_14	P34	DDR1_DQ<14>	M22	CPU2_M_CH1_MA_04 (60.61)
(60.61) CPU2_M_CH1_DQ_13	U36	DDR1_DQ<13>	L21	CPU2_M_CH1_MA_03 (60.61)
(60.61) CPU2_M_CH1_DQ_12	U35	DDR1_DQ<12>	K20	CPU2_M_CH1_MA_02 (60.61)
(60.61) CPU2_M_CH1_DQ_11	N35	DDR1_DQ<11>	L20	CPU2_M_CH1_MA_01 (60.61)
(60.61) CPU2_M_CH1_DQ_10	N36	DDR1_DQ<10>	K19	CPU2_M_CH1_MA_00 (60.61)
(60.61) CPU2_M_CH1_DQ_09	T36	DDR1_DQ<9>		
(60.61) CPU2_M_CH1_DQ_08	T35	DDR1_DQ<8>	G28	CPU2_M_CH1_ECC_7 (60.61)
(60.61) CPU2_M_CH1_DQ_07	Y36	DDR1_DQ<7>	H28	CPU2_M_CH1_ECC_6 (60.61)
(60.61) CPU2_M_CH1_DQ_06	Y35	DDR1_DQ<6>	H32	CPU2_M_CH1_ECC_5 (60.61)
(60.61) CPU2_M_CH1_DQ_05	AD35	DDR1_DQ<5>	H31	CPU2_M_CH1_ECC_4 (60.61)
(60.61) CPU2_M_CH1_DQ_04	AD34	DDR1_DQ<4>	G27	CPU2_M_CH1_ECC_3 (60.61)
(60.61) CPU2_M_CH1_DQ_03	W36	DDR1_DQ<3>	H27	CPU2_M_CH1_ECC_2 (60.61)
(60.61) CPU2_M_CH1_DQ_02	W35	DDR1_DQ<2>	G31	CPU2_M_CH1_ECC_1 (60.61)
(60.61) CPU2_M_CH1_DQ_01	AC35	DDR1_DQ<1>	G32	CPU2_M_CH1_ECC_0 (60.61)
(60.61) CPU2_M_CH1_DQ_00	AC34	DDR1_DQ<0>		
(61) CPU2_M_CH1_CS_7_N	J12	DDR1_CS_N<7>	H26	CPU2_M_CH1_CKE_3 (61)
(61) CPU2_M_CH1_CS_6_N	L12	DDR1_CS_N<6>	J25	CPU2_M_CH1_CKE_2 (61)
(61) CPU2_M_CH1_CS_5_N	H14	DDR1_CS_N<5>	J26	CPU2_M_CH1_CKE_1 (60)
(61) CPU2_M_CH1_CS_4_N	K15	DDR1_CS_N<4>	K25	CPU2_M_CH1_CKE_0 (60)
(60) CPU2_M_CH1_CS_3_N	K12	DDR1_CS_N<3>		
(60) CPU2_M_CH1_CS_2_N	L11	DDR1_CS_N<2>	J24	CPU2_M_CH1_BA_2 (60.61)
(60) CPU2_M_CH1_CS_1_N	L15	DDR1_CS_N<1>	L18	CPU2_M_CH1_BA_1 (60.61)
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(60) CPU2_M_CH1_CK_2_DN	H16	DDR1_RAS_N	K17	CPU2_M_CH1_RAS_N (60.61)
(61) CPU2_M_CH1_CK_1_DN	G19	DDR1_PAR_ERR_N	J21	CPU2_M_CH1_PERR_N (60.61)
(60) CPU2_M_CH1_CK_0_DN	H17	DDR1_CAS_N	K13	CPU2_M_CH1_CAS_N (60.61)
		DDR1_MA_PAR	J19	CPU2_M_CH1_MA_PAR (60.61)

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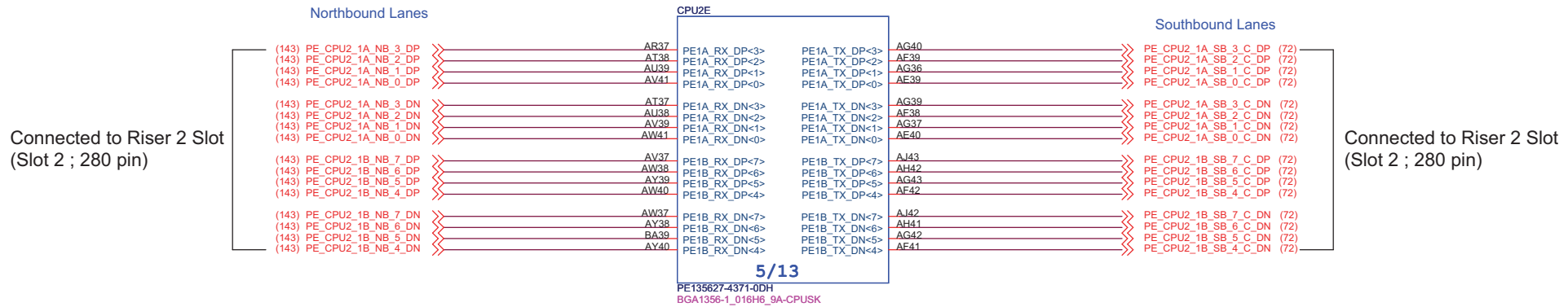
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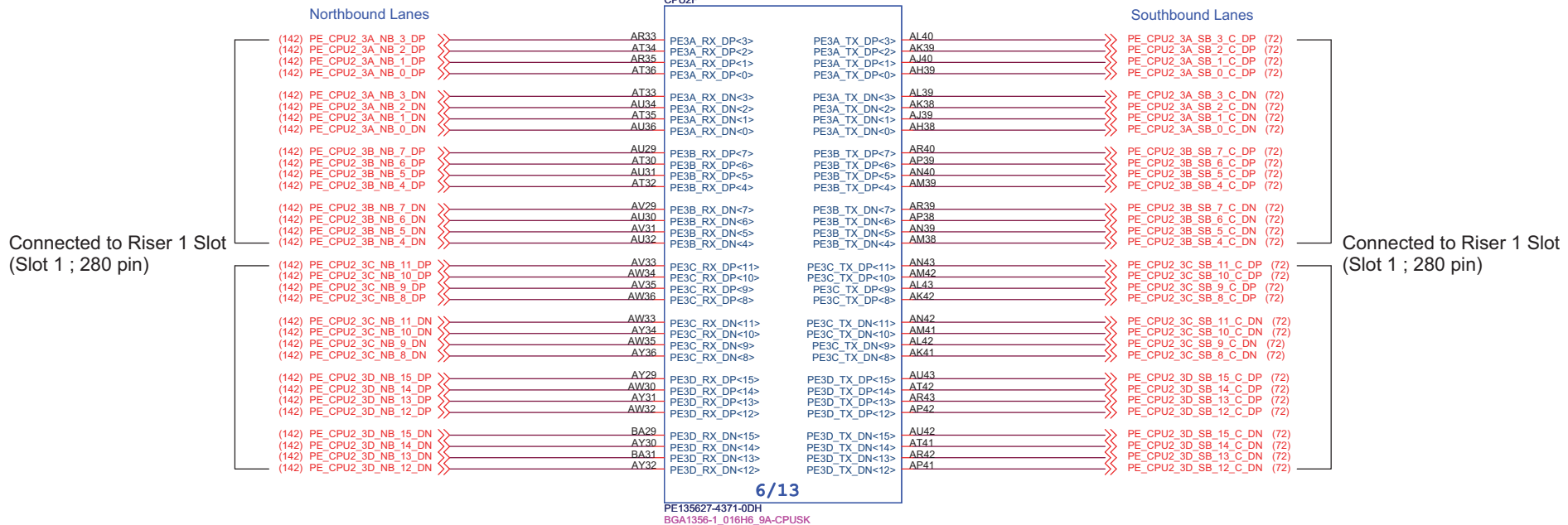
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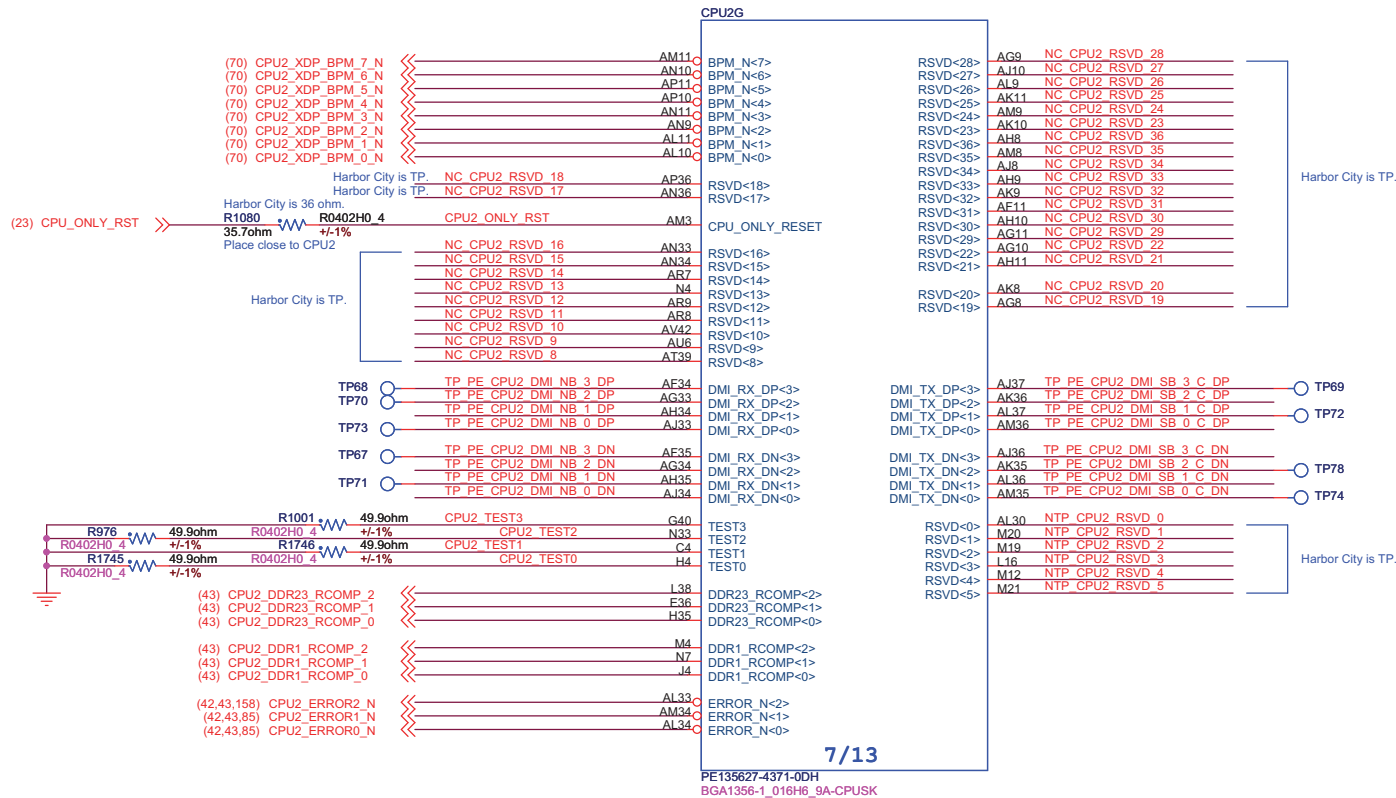
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(66.67) CPU2_M_CH3_DQ_62	U1	DDR3_DQ<62>	T2	CPU2_M_CH3_DQS_16_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_61	R3	DDR3_DQ<61>	K3	CPU2_M_CH3_DQS_15_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_60	P1	DDR3_DQ<60>	E2	CPU2_M_CH3_DQS_14_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_59	V3	DDR3_DQ<59>	A8	CPU2_M_CH3_DQS_13_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_58	V1	DDR3_DQ<58>	E43	CPU2_M_CH3_DQS_12_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_57	R1	DDR3_DQ<57>	K42	CPU2_M_CH3_DQS_11_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_56	R2	DDR3_DQ<56>	T41	CPU2_M_CH3_DQS_10_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_55	M1	DDR3_DQ<55>	AB42	CPU2_M_CH3_DQS_09_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_54	M2	DDR3_DQ<54>	A32	CPU2_M_CH3_DQS_08_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_53	J1	DDR3_DQ<53>	U3	CPU2_M_CH3_DQS_07_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_52	J3	DDR3_DQ<52>	L2	CPU2_M_CH3_DQS_06_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_51	N3	DDR3_DQ<51>	F1	CPU2_M_CH3_DQS_05_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_50	M3	DDR3_DQ<50>	B7	CPU2_M_CH3_DQS_04_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_49	K1	DDR3_DQ<49>	D42	CPU2_M_CH3_DQS_03_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_48	J2	DDR3_DQ<48>	J41	CPU2_M_CH3_DQS_02_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_47	G3	DDR3_DQ<47>	R42	CPU2_M_CH3_DQS_01_DP	(66.67)
(66.67) CPU2_M_CH3_DQ_46	F3	DDR3_DQ<46>	AA41	CPU2_M_CH3_DQS_00_DP	(66.67)
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(66.67) CPU2_M_CH3_DQ_43	G2	DDR3_DQ<43>	T1	CPU2_M_CH3_DQS_16_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_42	G1	DDR3_DQ<42>	L3	CPU2_M_CH3_DQS_15_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_41	D2	DDR3_DQ<41>	E1	CPU2_M_CH3_DQS_14_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_40	E3	DDR3_DQ<40>	B8	CPU2_M_CH3_DQS_13_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_39	B6	DDR3_DQ<39>	E42	CPU2_M_CH3_DQS_12_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_38	A6	DDR3_DQ<38>	K43	CPU2_M_CH3_DQS_11_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_37	B10	DDR3_DQ<37>	R41	CPU2_M_CH3_DQS_10_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_36	A10	DDR3_DQ<36>	AB43	CPU2_M_CH3_DQS_09_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_35	B4	DDR3_DQ<35>	T3	CPU2_M_CH3_DQS_08_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_34	B5	DDR3_DQ<34>	L1	CPU2_M_CH3_DQS_07_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_33	B9	DDR3_DQ<33>	F2	CPU2_M_CH3_DQS_06_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_32	A9	DDR3_DQ<32>	A7	CPU2_M_CH3_DQS_05_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_31	D41	DDR3_DQ<31>	D43	CPU2_M_CH3_DQS_04_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_30	C42	DDR3_DQ<30>	K41	CPU2_M_CH3_DQS_03_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_29	F43	DDR3_DQ<29>	R43	CPU2_M_CH3_DQS_02_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_28	F42	DDR3_DQ<28>	AB41	CPU2_M_CH3_DQS_01_DN	(66.67)
(66.67) CPU2_M_CH3_DQ_27	B41	DDR3_DQ<27>			
(66.67) CPU2_M_CH3_DQ_26	C41	DDR3_DQ<26>			
(66.67) CPU2_M_CH3_DQ_25	E41	DDR3_DQ<25>	A27	CPU2_M_CH3_MA_15	(66.67)
(66.67) CPU2_M_CH3_DQ_24	F41	DDR3_DQ<24>	C26	CPU2_M_CH3_MA_14	(66.67)
(66.67) CPU2_M_CH3_DQ_23	H42	DDR3_DQ<23>	D14	CPU2_M_CH3_MA_13	(66.67)
(66.67) CPU2_M_CH3_DQ_22	J43	DDR3_DQ<22>	B26	CPU2_M_CH3_MA_12	(66.67)
(66.67) CPU2_M_CH3_DQ_21	L41	DDR3_DQ<21>	A25	CPU2_M_CH3_MA_11	(66.67)
(66.67) CPU2_M_CH3_DQ_20	M41	DDR3_DQ<20>	A17	CPU2_M_CH3_MA_10	(66.67)
(66.67) CPU2_M_CH3_DQ_19	H41	DDR3_DQ<19>	B25	CPU2_M_CH3_MA_09	(66.67)
(66.67) CPU2_M_CH3_DQ_18	H43	DDR3_DQ<18>	B24	CPU2_M_CH3_MA_08	(66.67)
(66.67) CPU2_M_CH3_DQ_17	L42	DDR3_DQ<17>	D25	CPU2_M_CH3_MA_07	(66.67)
(66.67) CPU2_M_CH3_DQ_16	L43	DDR3_DQ<16>	C23	CPU2_M_CH3_MA_06	(66.67)
(66.67) CPU2_M_CH3_DQ_15	P42	DDR3_DQ<15>	C24	CPU2_M_CH3_MA_05	(66.67)
(66.67) CPU2_M_CH3_DQ_14	P43	DDR3_DQ<14>	D23	CPU2_M_CH3_MA_04	(66.67)
(66.67) CPU2_M_CH3_DQ_13	U43	DDR3_DQ<13>	C22	CPU2_M_CH3_MA_03	(66.67)
(66.67) CPU2_M_CH3_DQ_12	U41	DDR3_DQ<12>	D22	CPU2_M_CH3_MA_02	(66.67)
(66.67) CPU2_M_CH3_DQ_11	N43	DDR3_DQ<11>	D21	CPU2_M_CH3_MA_01	(66.67)
(66.67) CPU2_M_CH3_DQ_10	P41	DDR3_DQ<10>	C17	CPU2_M_CH3_MA_00	(66.67)
(66.67) CPU2_M_CH3_DQ_09	T43	DDR3_DQ<9>			
(66.67) CPU2_M_CH3_DQ_08	U42	DDR3_DQ<8>	A31	CPU2_M_CH3_ECC_7	(66.67)
(66.67) CPU2_M_CH3_DQ_07	W41	DDR3_DQ<7>	B31	CPU2_M_CH3_ECC_6	(66.67)
(66.67) CPU2_M_CH3_DQ_06	Y41	DDR3_DQ<6>	B35	CPU2_M_CH3_ECC_5	(66.67)
(66.67) CPU2_M_CH3_DQ_05	AD43	DDR3_DQ<5>	C35	CPU2_M_CH3_ECC_4	(66.67)
(66.67) CPU2_M_CH3_DQ_04	AD42	DDR3_DQ<4>	A30	CPU2_M_CH3_ECC_3	(66.67)
(66.67) CPU2_M_CH3_DQ_03	W43	DDR3_DQ<3>	B30	CPU2_M_CH3_ECC_2	(66.67)
(66.67) CPU2_M_CH3_DQ_02	W42	DDR3_DQ<2>	C33	CPU2_M_CH3_ECC_1	(66.67)
(66.67) CPU2_M_CH3_DQ_01	AC42	DDR3_DQ<1>	C34	CPU2_M_CH3_ECC_0	(66.67)
(66.67) CPU2_M_CH3_DQ_00	AC41	DDR3_DQ<0>			
(67) CPU2_M_CH3_CS_7_N	D12	DDR3_CS_N<7>	C28	CPU2_M_CH3_CKE_3	(67)
(67) CPU2_M_CH3_CS_6_N	C11	DDR3_CS_N<6>	A28	CPU2_M_CH3_CKE_2	(67)
(67) CPU2_M_CH3_CS_5_N	B14	DDR3_CS_N<5>	B29	CPU2_M_CH3_CKE_1	(66)
(67) CPU2_M_CH3_CS_4_N	A15	DDR3_CS_N<4>	B28	CPU2_M_CH3_CKE_0	(66)
(66) CPU2_M_CH3_CS_3_N	D11	DDR3_CS_N<3>			
(66) CPU2_M_CH3_CS_2_N	B11	DDR3_CS_N<2>	C27	CPU2_M_CH3_BA_2	(66.67)
(66) CPU2_M_CH3_CS_1_N	B13	DDR3_CS_N<1>	D17	CPU2_M_CH3_BA_1	(66.67)
(66) CPU2_M_CH3_CS_0_N	D16	DDR3_CS_N<0>	B16	CPU2_M_CH3_BA_0	(66.67)
(67) CPU2_M_CH3_CK_3_DP	C20	DDR3_CLK_DP<3>	C13	CPU2_M_CH3_ODT_3	(67)
(66) CPU2_M_CH3_CK_2_DP	B18	DDR3_CLK_DP<2>	C14	CPU2_M_CH3_ODT_2	(67)
(67) CPU2_M_CH3_CK_1_DP	B20	DDR3_CLK_DP<1>	C12	CPU2_M_CH3_ODT_1	(66)
(66) CPU2_M_CH3_CK_0_DP	C19	DDR3_CLK_DP<0>	D15	CPU2_M_CH3_ODT_0	(66)
(67) CPU2_M_CH3_CK_3_DN	C21	DDR3_CLK_DN<3>			
(66) CPU2_M_CH3_CK_2_DN	A18	DDR3_CLK_DN<2>	C16	CPU2_M_CH3_WE_N	(66.67)
(67) CPU2_M_CH3_CK_1_DN	A20	DDR3_CLK_DN<1>	A16	CPU2_M_CH3_RAS_N	(66.67)
(66) CPU2_M_CH3_CK_0_DN	B19	DDR3_CLK_DN<0>	A26	CPU2_M_CH3_PERR_N	(66.67)
			B15	CPU2_M_CH3_CAS_N	(66.67)
			C18	CPU2_M_CH3_MA_PAR	(66.67)

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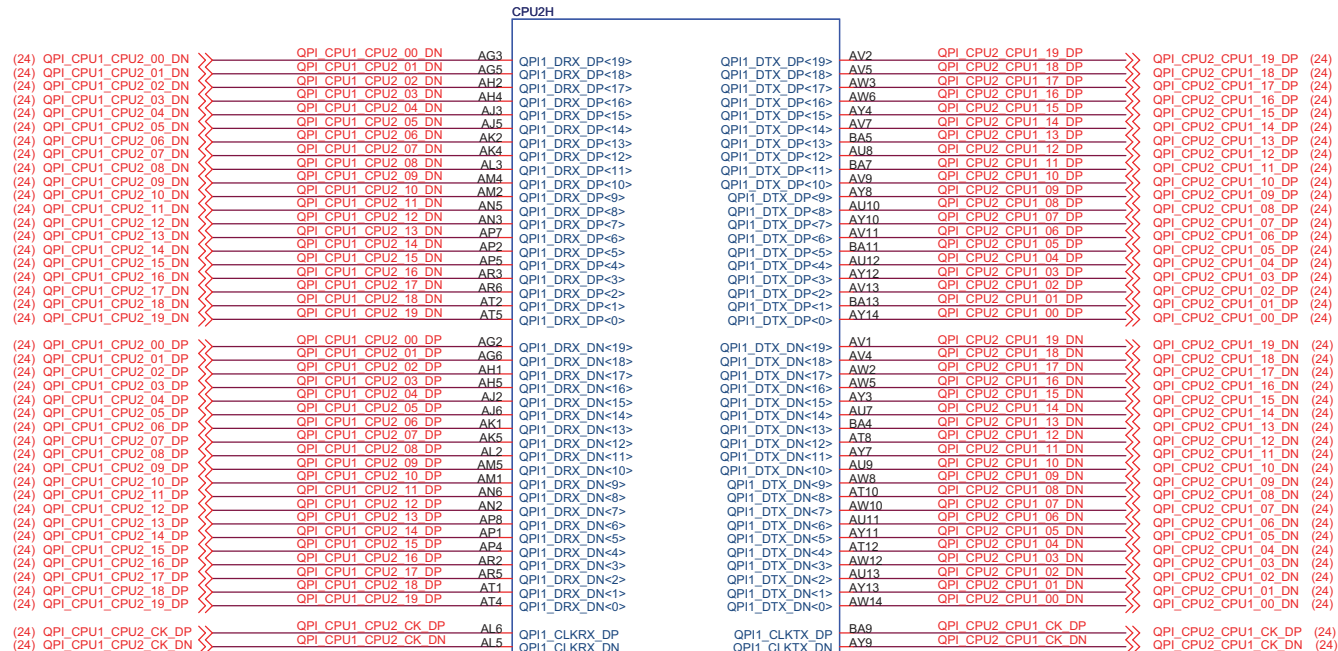
PE135627-4371-0DH
BGA1356-1_016H6_9A-CPU5K







Lane Reversed & DP\DN swapped on most lanes.(Reference Harbor City CRB Rev 1.0)
For routing need to redefine.

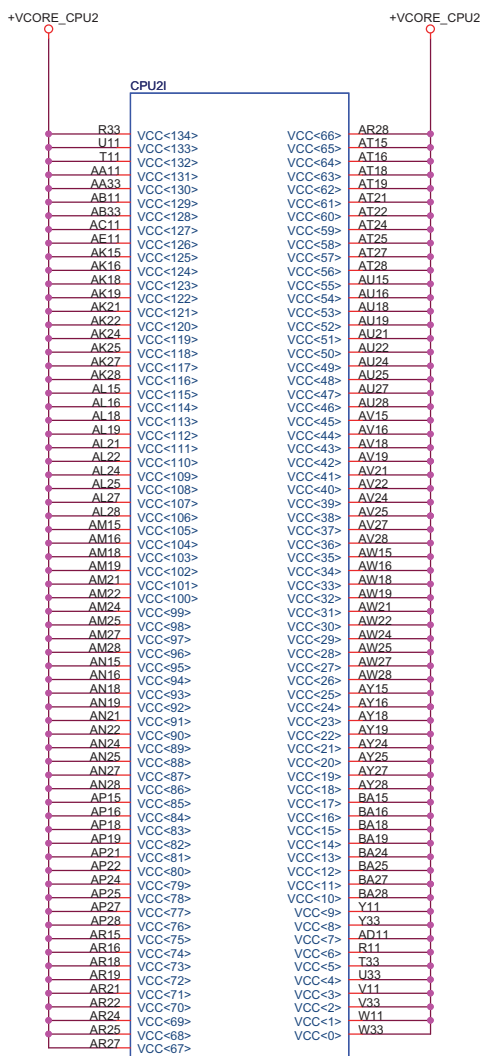


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PE135627-4371-00H
BGA1356-1_016H6_9A-CPUSK

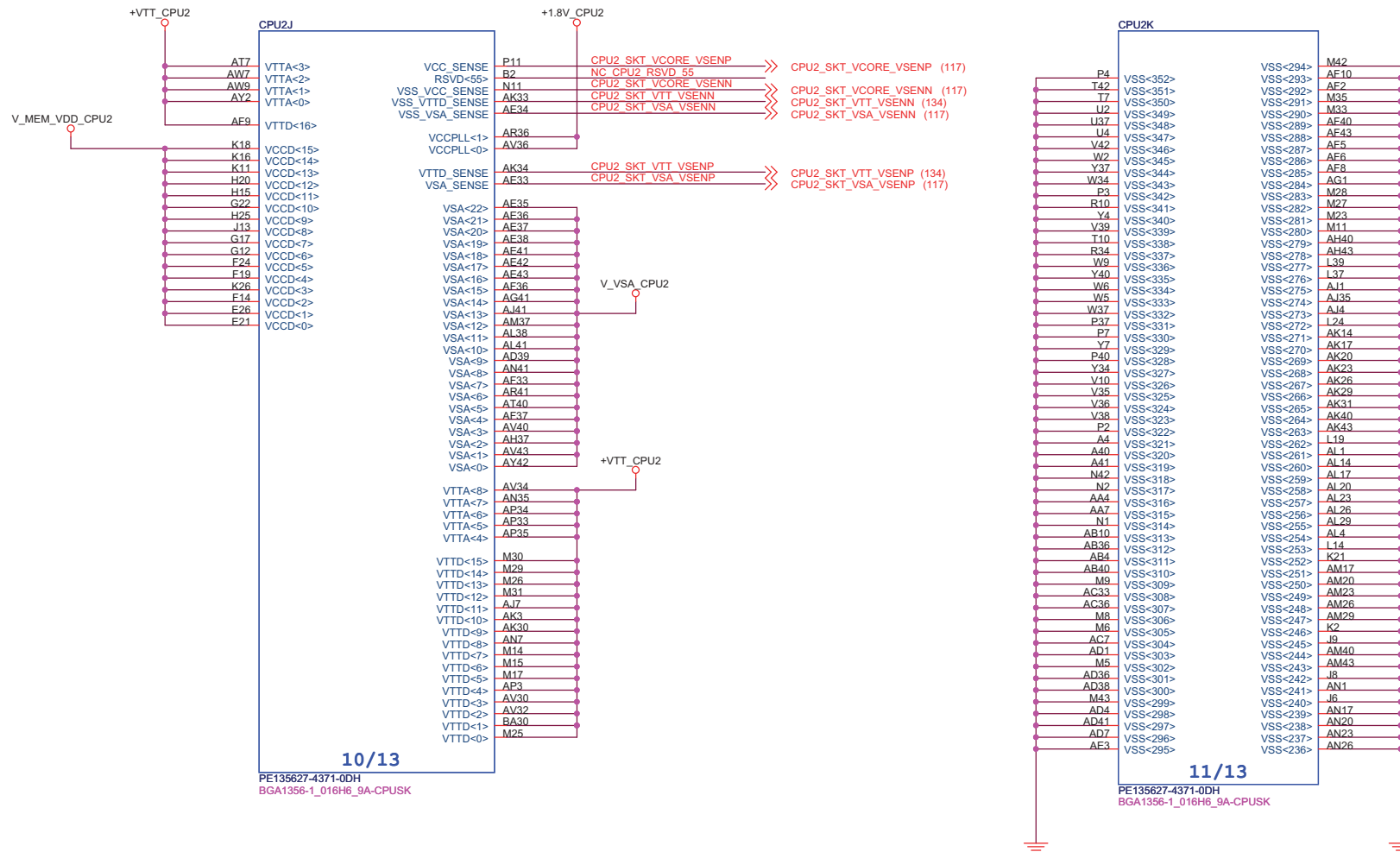
QPI LINK CONNECTIVITY (REFER TO HARBOR CITY CRB Rev1.0)

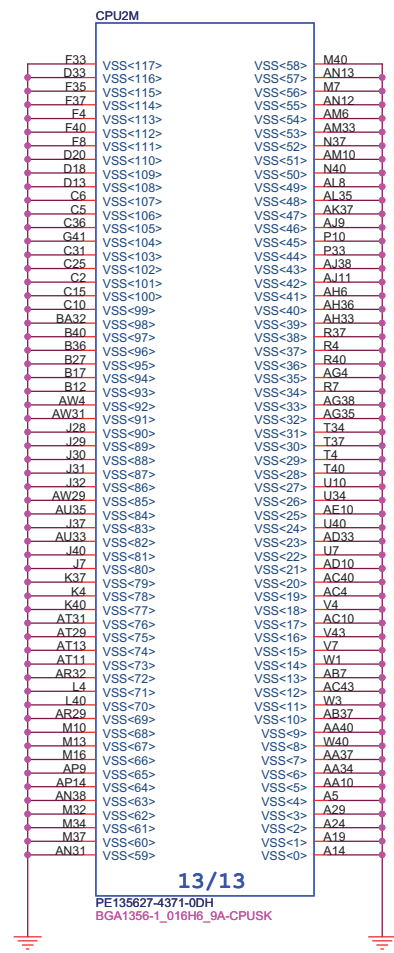
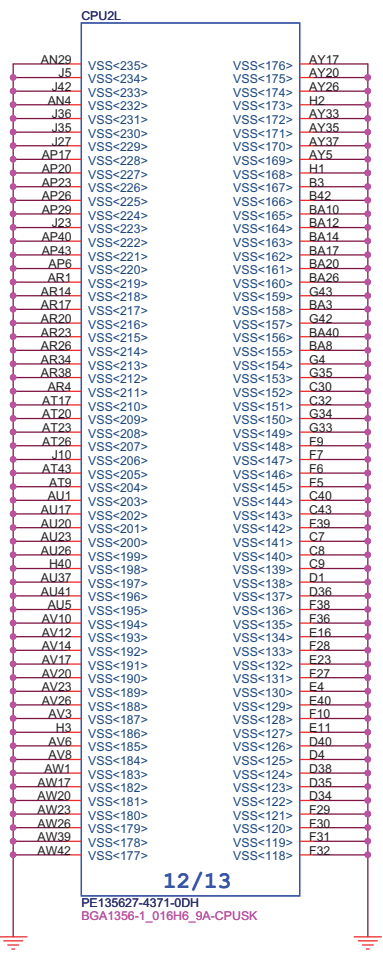
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QPI_CPU1_CPU2_DP(19..0)	QPI1_DTX_DP(19..0)	QPI1_DRX_DN(0..19)	YES-ALL LANES	YES-ALL LANES
QPI_CPU1_CPU2_DN(19..0)	QPI1_DTX_DN(19..0)	QPI1_DRX_DP(0..19)	YES-ALL LANES	YES-ALL LANES
QPI_CPU2_CPU1_DP(19..0)	QPI1_DRX_DN(0..19)	QPI1_DTX_DP(19..0)	YES-ALL LANES	YES-ALL LANES
QPI_CPU2_CPU1_DN(19..0)	QPI1_DRX_DP(0..19)	QPI1_DTX_DN(19..0)	YES-ALL LANES	YES-ALL LANES
BUS NAMING CONVENTION : TECHNOLOGY_FROM_TO POLARITY				
EXAMPLE : QPI_CPU1_CPU2_DP = QPI TECH, FROM CPU1, TO CPU2, DP POLARITY				

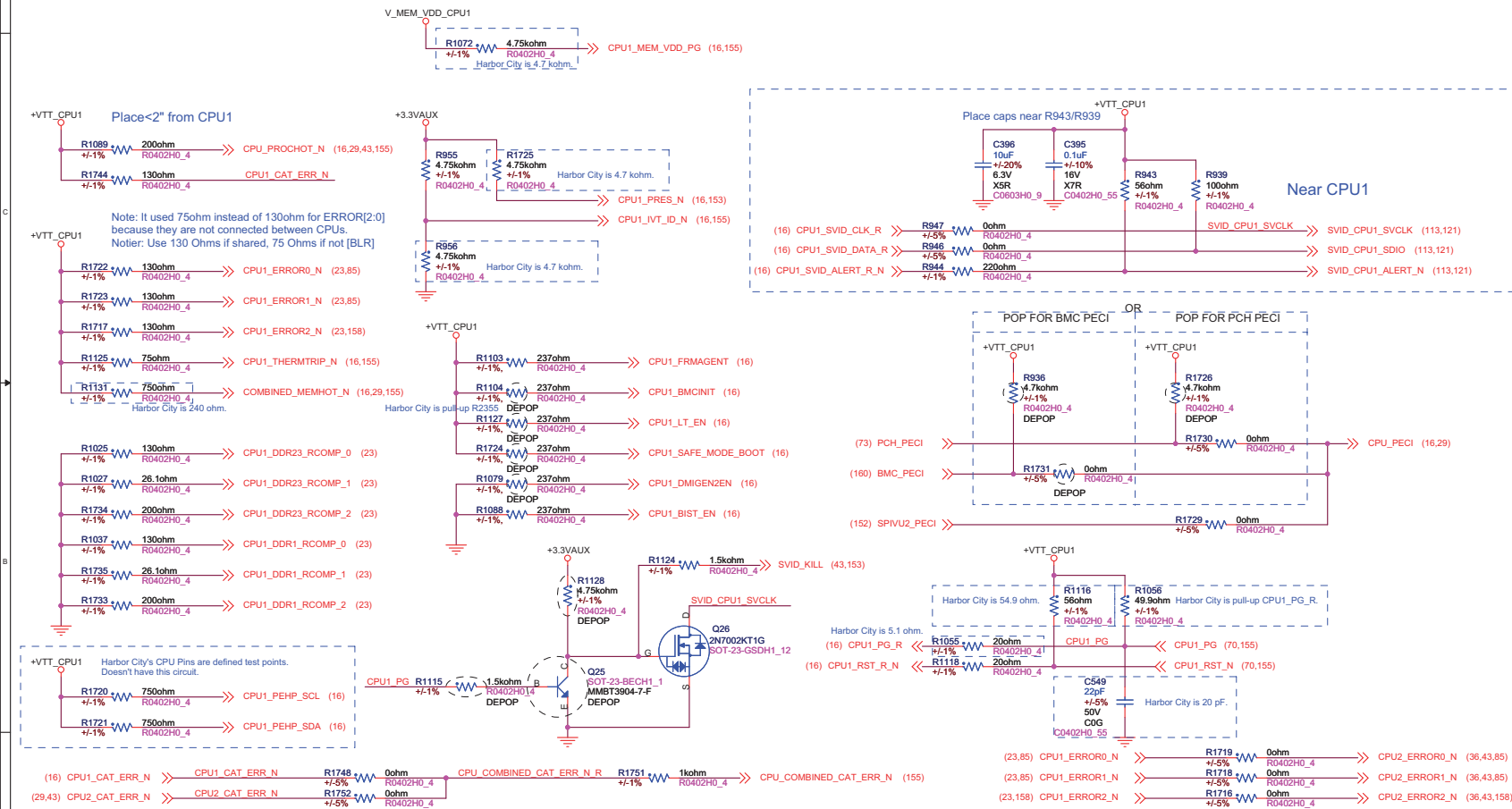


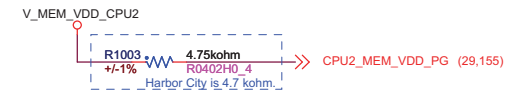
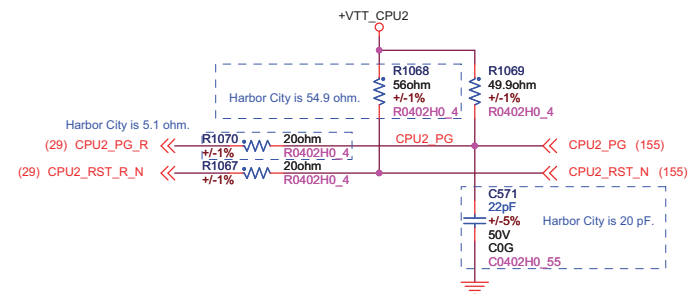
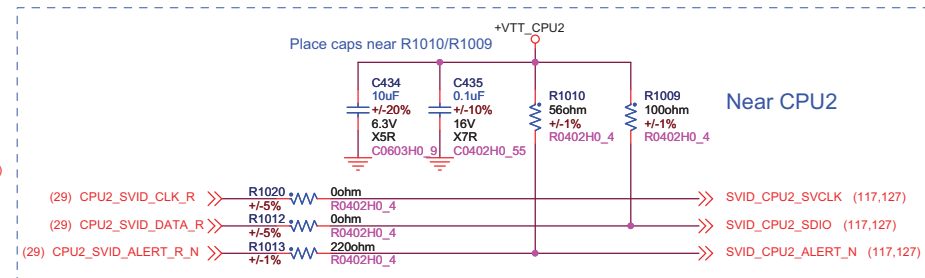
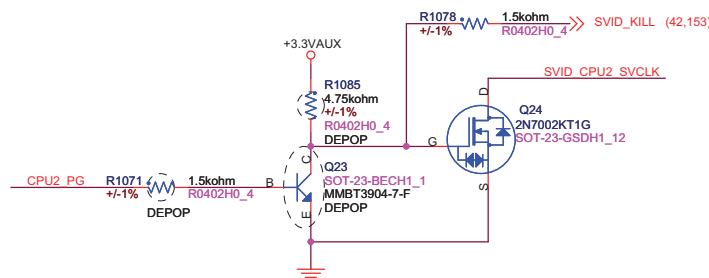
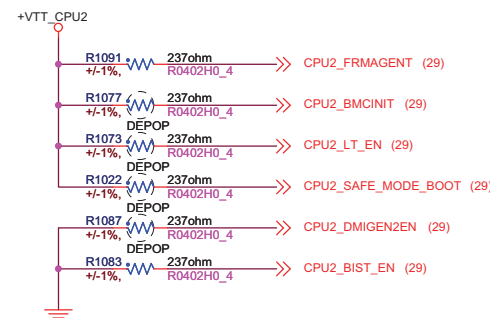
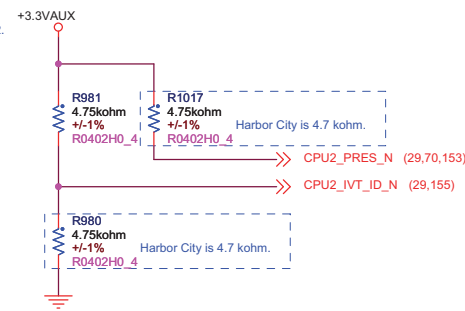
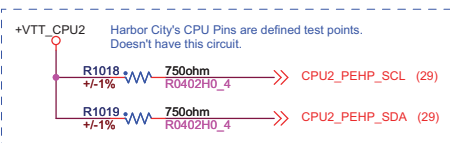
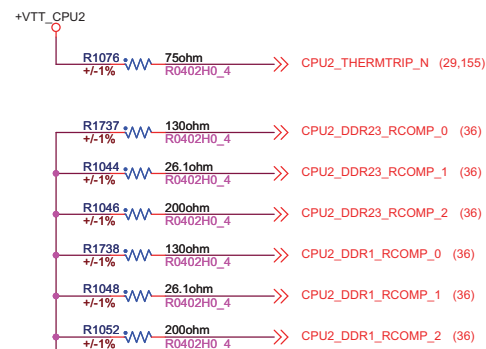
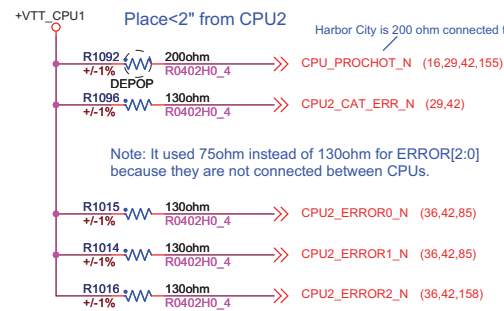
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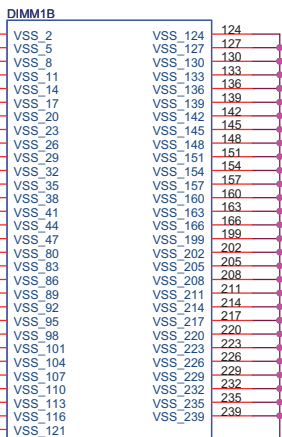
PE135627-4371-0DH
BGA1356-1_016H6_9A-CPU2K



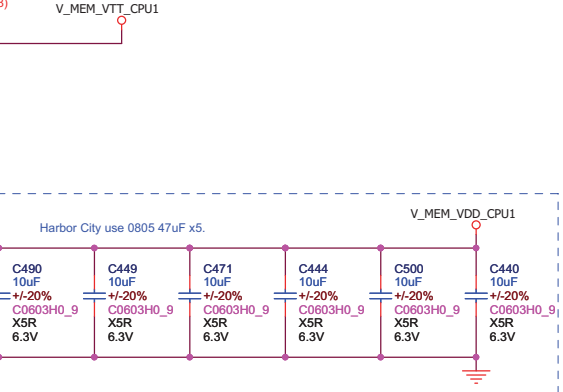
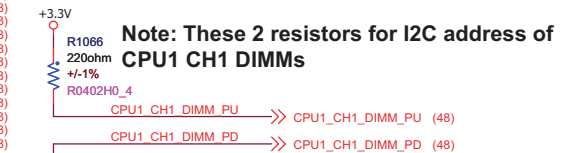








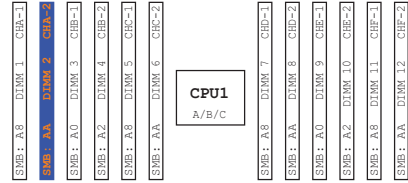
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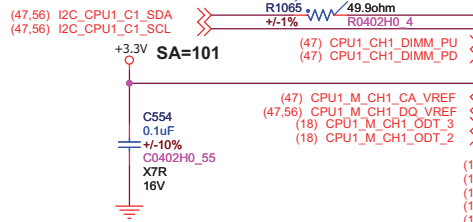
Hon Hai Precision Ind.Co., Ltd.

Document Number: PCB P/N: 01015C800-000-G 01/25/2011, 10:58 AM	Sheet 47 of 185	Rev X00
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DIMM population



Harbor City is connected to DIMM Slot Directly.



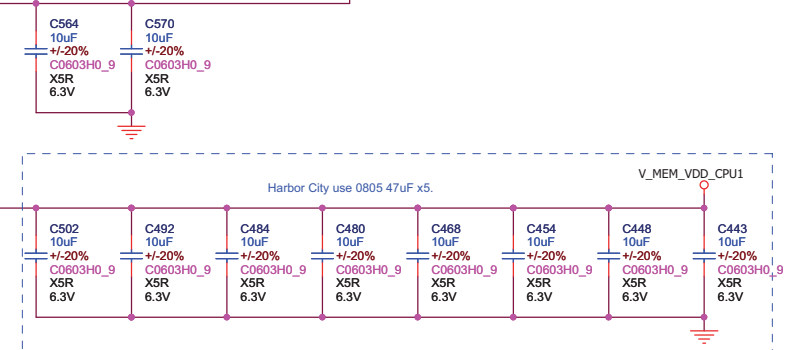
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(18,47) CPU1_M_CH1_BA_1	190	BA1	(18,47) CPU1_M_CH1_DQ_62	233	DO62
(18,47) CPU1_M_CH1_BA_0	71	BA0	(18,47) CPU1_M_CH1_DQ_61	228	DO61
(18,47) CPU1_M_CH1_MA_15	171	A15/NC	(18,47) CPU1_M_CH1_DQ_60	227	DO60
(18,47) CPU1_M_CH1_MA_14	172	A14	(18,47) CPU1_M_CH1_DQ_59	225	DO59
(18,47) CPU1_M_CH1_MA_13	173	A13	(18,47) CPU1_M_CH1_DQ_58	224	DO58
(18,47) CPU1_M_CH1_MA_12	174	A12/BC_N	(18,47) CPU1_M_CH1_DQ_57	223	DO57
(18,47) CPU1_M_CH1_MA_11	175	A11	(18,47) CPU1_M_CH1_DQ_56	222	DO56
(18,47) CPU1_M_CH1_MA_10	176	A10/AP	(18,47) CPU1_M_CH1_DQ_55	221	DO55
(18,47) CPU1_M_CH1_MA_09	177	A9	(18,47) CPU1_M_CH1_DQ_54	220	DO54
(18,47) CPU1_M_CH1_MA_08	178	A8	(18,47) CPU1_M_CH1_DQ_53	219	DO53
(18,47) CPU1_M_CH1_MA_07	179	A7	(18,47) CPU1_M_CH1_DQ_52	218	DO52
(18,47) CPU1_M_CH1_MA_06	180	A6	(18,47) CPU1_M_CH1_DQ_51	217	DO51
(18,47) CPU1_M_CH1_MA_05	181	A5	(18,47) CPU1_M_CH1_DQ_50	216	DO50
(18,47) CPU1_M_CH1_MA_04	182	A4	(18,47) CPU1_M_CH1_DQ_49	215	DO49
(18,47) CPU1_M_CH1_MA_03	183	A3	(18,47) CPU1_M_CH1_DQ_48	214	DO48
(18,47) CPU1_M_CH1_MA_02	184	A2	(18,47) CPU1_M_CH1_DQ_47	213	DO47
(18,47) CPU1_M_CH1_MA_01	185	A1	(18,47) CPU1_M_CH1_DQ_46	212	DO46
(18,47) CPU1_M_CH1_MA_00	186	A0	(18,47) CPU1_M_CH1_DQ_45	211	DO45
(18) CPU1_M_CH1_CS_7_N	198	S3_N/NC	(18,47) CPU1_M_CH1_DQ_44	210	DO44
(18) CPU1_M_CH1_CS_6_N	79	S2_N/NC	(18,47) CPU1_M_CH1_DQ_43	209	DO43
(18) CPU1_M_CH1_CS_5_N	76	S1_N/NC	(18,47) CPU1_M_CH1_DQ_42	208	DO42
(18) CPU1_M_CH1_CS_4_N	193	S0_N	(18,47) CPU1_M_CH1_DQ_41	207	DO41
(18,47) CPU1_M_CH1_RAS_N	192	RAS_N	(18,47) CPU1_M_CH1_DQ_40	206	DO40
(18,47) CPU1_M_CH1_CAS_N	74	CAS_N	(18,47) CPU1_M_CH1_DQ_39	205	DO39
(18,47) CPU1_M_CH1_WE_N	63	WE_N	(18,47) CPU1_M_CH1_DQ_38	204	DO38
(18) CPU1_M_CH1_CK_3_DP	64	CK_3	(18,47) CPU1_M_CH1_DQ_37	203	DO37
(18) CPU1_M_CH1_CK_3_DN	65	CK_3	(18,47) CPU1_M_CH1_DQ_36	202	DO36
(18) CPU1_M_CH1_CK_1_DP	185	CK_1	(18,47) CPU1_M_CH1_DQ_35	201	DO35
(18) CPU1_M_CH1_CK_1_DN	186	CK_1	(18,47) CPU1_M_CH1_DQ_34	200	DO34
(18) CPU1_M_CH1_CKE_3	187	CKE_3	(18,47) CPU1_M_CH1_DQ_33	199	DO33
(18) CPU1_M_CH1_CKE_2	50	CKE_2	(18,47) CPU1_M_CH1_DQ_32	198	DO32
(18) CPU1_M_CH1_CKE_1	51	CKE_1	(18,47) CPU1_M_CH1_DQ_31	197	DO31
(18) CPU1_M_CH1_CKE_0	52	CKE_0	(18,47) CPU1_M_CH1_DQ_30	196	DO30
(18,47) CPU1_M_CH1_ECC_7	165	CB7/NC	(18,47) CPU1_M_CH1_DQ_29	195	DO29
(18,47) CPU1_M_CH1_ECC_6	166	CB6/NC	(18,47) CPU1_M_CH1_DQ_28	194	DO28
(18,47) CPU1_M_CH1_ECC_5	167	CB5/NC	(18,47) CPU1_M_CH1_DQ_27	193	DO27
(18,47) CPU1_M_CH1_ECC_4	168	CB4/NC	(18,47) CPU1_M_CH1_DQ_26	192	DO26
(18,47) CPU1_M_CH1_ECC_3	169	CB3/NC	(18,47) CPU1_M_CH1_DQ_25	191	DO25
(18,47) CPU1_M_CH1_ECC_2	170	CB2/NC	(18,47) CPU1_M_CH1_DQ_24	190	DO24
(18,47) CPU1_M_CH1_ECC_1	171	CB1/NC	(18,47) CPU1_M_CH1_DQ_23	189	DO23
(18,47) CPU1_M_CH1_ECC_0	172	CB0/NC	(18,47) CPU1_M_CH1_DQ_22	188	DO22
(18,47) CPU1_M_CH1_DQS_17_DN	162	NC/DQS17_N/TDQS17_N	(18,47) CPU1_M_CH1_DQ_21	187	DO21
(18,47) CPU1_M_CH1_DQS_17_DP	163	DM8/DQS17/TDQS17/NC	(18,47) CPU1_M_CH1_DQ_20	186	DO20
(18,47) CPU1_M_CH1_DQS_16_DN	231	NC/DQS16_N/TDQS16_N	(18,47) CPU1_M_CH1_DQ_19	185	DO19
(18,47) CPU1_M_CH1_DQS_16_DP	232	DM7/DQS16/TDQS16/NC	(18,47) CPU1_M_CH1_DQ_18	184	DO18
(18,47) CPU1_M_CH1_DQS_15_DN	222	NC/DQS15_N/TDQS15_N	(18,47) CPU1_M_CH1_DQ_17	183	DO17
(18,47) CPU1_M_CH1_DQS_15_DP	223	DM6/DQS15/TDQS15/NC	(18,47) CPU1_M_CH1_DQ_16	182	DO16
(18,47) CPU1_M_CH1_DQS_14_DN	213	NC/DQS14_N/TDQS14_N	(18,47) CPU1_M_CH1_DQ_15	181	DO15
(18,47) CPU1_M_CH1_DQS_14_DP	214	DM5/DQS14/TDQS14/NC	(18,47) CPU1_M_CH1_DQ_14	180	DO14
(18,47) CPU1_M_CH1_DQS_13_DN	204	NC/DQS13_N/TDQS13_N	(18,47) CPU1_M_CH1_DQ_13	179	DO13
(18,47) CPU1_M_CH1_DQS_13_DP	205	DM4/DQS13/TDQS13/NC	(18,47) CPU1_M_CH1_DQ_12	178	DO12
(18,47) CPU1_M_CH1_DQS_12_DN	152	NC/DQS12_N/TDQS12_N	(18,47) CPU1_M_CH1_DQ_11	177	DO11
(18,47) CPU1_M_CH1_DQS_12_DP	153	DM3/DQS12/TDQS12/NC	(18,47) CPU1_M_CH1_DQ_10	176	DO10
(18,47) CPU1_M_CH1_DQS_11_DN	144	NC/DQS11_N/TDQS11_N	(18,47) CPU1_M_CH1_DQ_09	175	DO09
(18,47) CPU1_M_CH1_DQS_11_DP	145	DM2/DQS11/TDQS11/NC	(18,47) CPU1_M_CH1_DQ_08	174	DO08
(18,47) CPU1_M_CH1_DQS_10_DN	135	NC/DQS10_N/TDQS10_N	(18,47) CPU1_M_CH1_DQ_07	173	DO07
(18,47) CPU1_M_CH1_DQS_10_DP	136	DM1/DQS10/TDQS10/NC	(18,47) CPU1_M_CH1_DQ_06	172	DO06
(18,47) CPU1_M_CH1_DQS_09_DN	126	NC/DQS9_N/TDQS9_N	(18,47) CPU1_M_CH1_DQ_05	171	DO05
(18,47) CPU1_M_CH1_DQS_09_DP	127	DM0/DQS9/TDQS9/NC	(18,47) CPU1_M_CH1_DQ_04	170	DO04
(18,47) CPU1_M_CH1_DQS_08_DN	42	DQS8_N	(18,47) CPU1_M_CH1_DQ_03	169	DO03
(18,47) CPU1_M_CH1_DQS_08_DP	43	DQS8_N	(18,47) CPU1_M_CH1_DQ_02	168	DO02
(18,47) CPU1_M_CH1_DQS_07_DN	111	DQS7_N	(18,47) CPU1_M_CH1_DQ_01	167	DO01
(18,47) CPU1_M_CH1_DQS_07_DP	112	DQS7_N	(18,47) CPU1_M_CH1_DQ_00	166	DO00
(18,47) CPU1_M_CH1_DQS_06_DN	102	DQS6_N			
(18,47) CPU1_M_CH1_DQS_06_DP	103	DQS6_N			
(18,47) CPU1_M_CH1_DQS_05_DN	93	DQS5_N			
(18,47) CPU1_M_CH1_DQS_05_DP	94	DQS5_N			
(18,47) CPU1_M_CH1_DQS_04_DN	84	DQS4_N			
(18,47) CPU1_M_CH1_DQS_04_DP	85	DQS4_N			
(18,47) CPU1_M_CH1_DQS_03_DN	33	DQS3_N			
(18,47) CPU1_M_CH1_DQS_03_DP	34	DQS3_N			
(18,47) CPU1_M_CH1_DQS_02_DN	24	DQS2_N			
(18,47) CPU1_M_CH1_DQS_02_DP	25	DQS2_N			
(18,47) CPU1_M_CH1_DQS_01_DN	15	DQS1_N			
(18,47) CPU1_M_CH1_DQS_01_DP	16	DQS1_N			
(18,47) CPU1_M_CH1_DQS_00_DN	6	DQS0_N			
(18,47) CPU1_M_CH1_DQS_00_DP	7	DQS0_N			
(18,47) CPU1_M_CH1_PERR_N	53	ERR_OUT_N/NC			
(18,47) CPU1_M_CH1_MA_PAR	68	PAR_IN/NC			
(18,47) CPU1_M_CH1_MA_PAR	167	NC/TEST			

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SPD = 0xAA
TSOD = 0x3A

EVENT_N/NC
RESET_N

DIMM_TEMP_EVENT_N (47,50,51,53,54,60,61,63,64,66,67,153)
CPU1_M_CH1_RST_N (16,47)



FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)

Hon Hai Precision Ind. Co., Ltd.

Title
CPU1 CH1 DIMM1

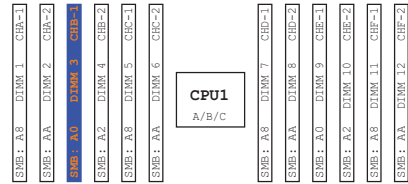
Document Number:
PCB P/N: 01015C800-000-G

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01/25/2011, 10:58 AM

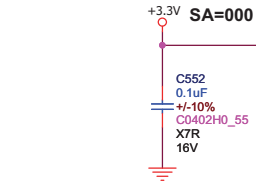
DIMM population



(51,53,54,56) I2C_CPU1_C23_SDA
(51,53,54,56) I2C_CPU1_C23_SCL

Harbor City is connected to DIMM Slot Directly.

R1058 49.9ohm
R0402H0_4



(47,51) CPU1_M_CH2_CA_VREF
(51,56) CPU1_M_CH2_DQ_VREF
(19) CPU1_M_CH2_ODT_0
(19) CPU1_M_CH2_ODT_0

(19,51) CPU1_M_CH2_ECC_7
(19,51) CPU1_M_CH2_ECC_6
(19,51) CPU1_M_CH2_ECC_5
(19,51) CPU1_M_CH2_ECC_4
(19,51) CPU1_M_CH2_ECC_3
(19,51) CPU1_M_CH2_ECC_2
(19,51) CPU1_M_CH2_ECC_1
(19,51) CPU1_M_CH2_ECC_0

(19,51) CPU1_M_CH2_DQS_17_DN
(19,51) CPU1_M_CH2_DQS_17_DP
(19,51) CPU1_M_CH2_DQS_16_DN
(19,51) CPU1_M_CH2_DQS_16_DP
(19,51) CPU1_M_CH2_DQS_15_DN
(19,51) CPU1_M_CH2_DQS_15_DP
(19,51) CPU1_M_CH2_DQS_14_DN
(19,51) CPU1_M_CH2_DQS_14_DP
(19,51) CPU1_M_CH2_DQS_13_DN
(19,51) CPU1_M_CH2_DQS_13_DP
(19,51) CPU1_M_CH2_DQS_12_DN
(19,51) CPU1_M_CH2_DQS_12_DP
(19,51) CPU1_M_CH2_DQS_11_DN
(19,51) CPU1_M_CH2_DQS_11_DP
(19,51) CPU1_M_CH2_DQS_10_DN
(19,51) CPU1_M_CH2_DQS_10_DP
(19,51) CPU1_M_CH2_DQS_09_DN
(19,51) CPU1_M_CH2_DQS_09_DP
(19,51) CPU1_M_CH2_DQS_08_DN
(19,51) CPU1_M_CH2_DQS_08_DP
(19,51) CPU1_M_CH2_DQS_07_DN
(19,51) CPU1_M_CH2_DQS_07_DP
(19,51) CPU1_M_CH2_DQS_06_DN
(19,51) CPU1_M_CH2_DQS_06_DP
(19,51) CPU1_M_CH2_DQS_05_DN
(19,51) CPU1_M_CH2_DQS_05_DP
(19,51) CPU1_M_CH2_DQS_04_DN
(19,51) CPU1_M_CH2_DQS_04_DP
(19,51) CPU1_M_CH2_DQS_03_DN
(19,51) CPU1_M_CH2_DQS_03_DP
(19,51) CPU1_M_CH2_DQS_02_DN
(19,51) CPU1_M_CH2_DQS_02_DP
(19,51) CPU1_M_CH2_DQS_01_DN
(19,51) CPU1_M_CH2_DQS_01_DP
(19,51) CPU1_M_CH2_DQS_00_DN
(19,51) CPU1_M_CH2_DQS_00_DP

(19,51) CPU1_M_CH2_PERR_N
(19,51) CPU1_M_CH2_MA_PARR

NC_CPU1_CH2_D0_P167
NC_TEST

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SPD = 0xA0
TSOD = 0x30

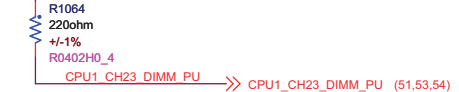
EVENT_NNC
RESET_N

DIMM_TEMP_EVENT_N (47,48,51,53,54,60,61,63,64,66,67,153)
CPU1_M_CH23_RST_N (16,51,53,54)



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Note: These 2 resistors for I2C address of CPU1 CH23 DIMMs

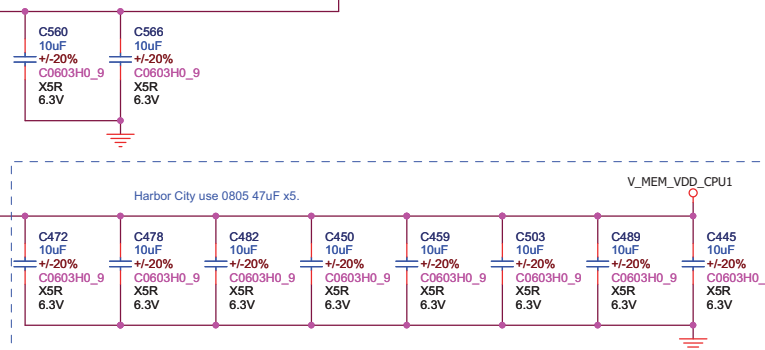


CPU1_CH23_DIMM_PD (51,53,54)



CPU1_CH23_DIMM_PD (51,53,54)

V_MEM_VTT_CPU1



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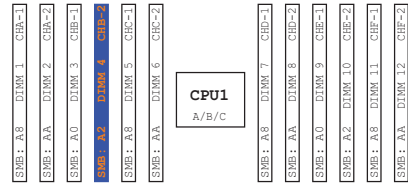
Hon Hai Precision Ind. Co., Ltd.

Title
CPU1 CH2 DIMM0

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PCB P/N: 01015C800-000-G
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DIMM population



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(50,53,54,56) I2C_CPU1_C23_SDA
(50,53,54,56) I2C_CPU1_C23_SCL

+3.3V SA=001

C556
0.1uF
+/-10%
C0402H0_55
X7R
16V

(19,50) CPU1_M_CH2_BA_2	>>>	52	B2	DQ63	234	CPU1_M_CH2_DQ_63	(19,50)
(19,50) CPU1_M_CH2_BA_1	>>>	190	BA1	DQ62	233	CPU1_M_CH2_DQ_62	(19,50)
(19,50) CPU1_M_CH2_BA_0	>>>	71	BA0	DQ61	228	CPU1_M_CH2_DQ_61	(19,50)
(19,50) CPU1_M_CH2_MA_15	>>>	171	A15/NC	DQ60	227	CPU1_M_CH2_DQ_60	(19,50)
(19,50) CPU1_M_CH2_MA_14	>>>	172	A14	DQ59	114	CPU1_M_CH2_DQ_59	(19,50)
(19,50) CPU1_M_CH2_MA_13	>>>	173	A13	DQ58	109	CPU1_M_CH2_DQ_58	(19,50)
(19,50) CPU1_M_CH2_MA_12	>>>	55	A12_BC_N	DQ57	108	CPU1_M_CH2_DQ_57	(19,50)
(19,50) CPU1_M_CH2_MA_11	>>>	70	A11	DQ56	225	CPU1_M_CH2_DQ_56	(19,50)
(19,50) CPU1_M_CH2_MA_10	>>>	175	A10/AP	DQ55	224	CPU1_M_CH2_DQ_55	(19,50)
(19,50) CPU1_M_CH2_MA_09	>>>	176	A9	DQ54	219	CPU1_M_CH2_DQ_54	(19,50)
(19,50) CPU1_M_CH2_MA_08	>>>	177	A8	DQ53	218	CPU1_M_CH2_DQ_53	(19,50)
(19,50) CPU1_M_CH2_MA_07	>>>	178	A7	DQ52	106	CPU1_M_CH2_DQ_52	(19,50)
(19,50) CPU1_M_CH2_MA_06	>>>	58	A6	DQ51	105	CPU1_M_CH2_DQ_51	(19,50)
(19,50) CPU1_M_CH2_MA_05	>>>	59	A5	DQ50	100	CPU1_M_CH2_DQ_50	(19,50)
(19,50) CPU1_M_CH2_MA_04	>>>	180	A4	DQ49	99	CPU1_M_CH2_DQ_49	(19,50)
(19,50) CPU1_M_CH2_MA_03	>>>	61	A3	DQ48	216	CPU1_M_CH2_DQ_48	(19,50)
(19,50) CPU1_M_CH2_MA_02	>>>	181	A2	DQ46	215	CPU1_M_CH2_DQ_46	(19,50)
(19,50) CPU1_M_CH2_MA_01	>>>	188	A1	DQ45	210	CPU1_M_CH2_DQ_45	(19,50)
(19,50) CPU1_M_CH2_MA_00	>>>	188	A0	DQ44	209	CPU1_M_CH2_DQ_44	(19,50)
(19) CPU1_M_CH2_CS_7_N	>>>	198	S3_N/NC	DQ43	96	CPU1_M_CH2_DQ_43	(19,50)
(19) CPU1_M_CH2_CS_6_N	>>>	79	S2_N/NC	DQ42	91	CPU1_M_CH2_DQ_42	(19,50)
(19) CPU1_M_CH2_CS_5_N	>>>	76	S1_N/NC	DQ41	90	CPU1_M_CH2_DQ_41	(19,50)
(19) CPU1_M_CH2_CS_4_N	>>>	193	S0_N	DQ40	207	CPU1_M_CH2_DQ_40	(19,50)
(19,50) CPU1_M_CH2_RAS_N	>>>	192	RAS_N	DQ39	206	CPU1_M_CH2_DQ_39	(19,50)
(19,50) CPU1_M_CH2_CAS_N	>>>	74	CAS_N	DQ38	201	CPU1_M_CH2_DQ_38	(19,50)
(19,50) CPU1_M_CH2_WE_N	>>>	63	WE_N	DQ37	200	CPU1_M_CH2_DQ_37	(19,50)
(19) CPU1_M_CH2_CK_3_DP	>>>	64	CK_3	DQ36	88	CPU1_M_CH2_DQ_36	(19,50)
(19) CPU1_M_CH2_CK_3_DN	>>>	185	CK_3_N	DQ35	87	CPU1_M_CH2_DQ_35	(19,50)
(19) CPU1_M_CH2_CK_1_DP	>>>	184	CK_1	DQ34	82	CPU1_M_CH2_DQ_34	(19,50)
(19) CPU1_M_CH2_CK_1_DN	>>>	169	CKE1/NC	DQ33	81	CPU1_M_CH2_DQ_33	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	50	CKE0	DQ31	156	CPU1_M_CH2_DQ_31	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	238	SDA	DQ30	155	CPU1_M_CH2_DQ_30	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	118	SCL	DQ29	149	CPU1_M_CH2_DQ_29	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	119	SA2	DQ28	37	CPU1_M_CH2_DQ_28	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	237	SA1	DQ27	36	CPU1_M_CH2_DQ_27	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	117	SA0	DQ26	31	CPU1_M_CH2_DQ_26	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	236	VDDSPD	DQ25	30	CPU1_M_CH2_DQ_25	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	67	VREFCA	DQ24	147	CPU1_M_CH2_DQ_24	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	1	VREFDQ	DQ23	146	CPU1_M_CH2_DQ_23	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	195	ODT1/NC	DQ22	141	CPU1_M_CH2_DQ_22	(19,50)
(19) CPU1_M_CH2_CKE_2	>>>	165	ODT0	DQ21	140	CPU1_M_CH2_DQ_21	(19,50)
(19,50) CPU1_M_CH2_ECC_7	>>>	164	CB7/NC	DQ20	28	CPU1_M_CH2_DQ_20	(19,50)
(19,50) CPU1_M_CH2_ECC_6	>>>	159	CB6/NC	DQ19	27	CPU1_M_CH2_DQ_19	(19,50)
(19,50) CPU1_M_CH2_ECC_5	>>>	158	CB5/NC	DQ18	22	CPU1_M_CH2_DQ_18	(19,50)
(19,50) CPU1_M_CH2_ECC_4	>>>	157	CB4/NC	DQ17	21	CPU1_M_CH2_DQ_17	(19,50)
(19,50) CPU1_M_CH2_ECC_3	>>>	45	CB3/NC	DQ16	138	CPU1_M_CH2_DQ_16	(19,50)
(19,50) CPU1_M_CH2_ECC_2	>>>	40	CB2/NC	DQ15	137	CPU1_M_CH2_DQ_15	(19,50)
(19,50) CPU1_M_CH2_ECC_1	>>>	39	CB1/NC	DQ14	132	CPU1_M_CH2_DQ_14	(19,50)
(19,50) CPU1_M_CH2_ECC_0	>>>	162	CB0/NC	DQ13	131	CPU1_M_CH2_DQ_13	(19,50)
(19,50) CPU1_M_CH2_DQS_17_DN	>>>	161	NC/DQS17_N/TDQS17_N	DQ12	11	CPU1_M_CH2_DQ_12	(19,50)
(19,50) CPU1_M_CH2_DQS_17_DP	>>>	231	DM8/DQS17/TDQS17/NC	DQ11	18	CPU1_M_CH2_DQ_11	(19,50)
(19,50) CPU1_M_CH2_DQS_16_DN	>>>	230	NC/DQS16_N/TDQS16_N	DQ10	13	CPU1_M_CH2_DQ_10	(19,50)
(19,50) CPU1_M_CH2_DQS_16_DP	>>>	229	DM7/DQS16/TDQS16/NC	DQ9	12	CPU1_M_CH2_DQ_09	(19,50)
(19,50) CPU1_M_CH2_DQS_15_DN	>>>	228	NC/DQS15_N/TDQS15_N	DQ8	129	CPU1_M_CH2_DQ_08	(19,50)
(19,50) CPU1_M_CH2_DQS_15_DP	>>>	227	DM6/DQS15/TDQS15	DQ7	128	CPU1_M_CH2_DQ_07	(19,50)
(19,50) CPU1_M_CH2_DQS_14_DN	>>>	226	NC/DQS14_N/TDQS14_N	DQ6	123	CPU1_M_CH2_DQ_06	(19,50)
(19,50) CPU1_M_CH2_DQS_14_DP	>>>	225	DM5/DQS14/TDQS14	DQ5	122	CPU1_M_CH2_DQ_05	(19,50)
(19,50) CPU1_M_CH2_DQS_13_DN	>>>	224	NC/DQS13_N/TDQS13_N	DQ4	10	CPU1_M_CH2_DQ_04	(19,50)
(19,50) CPU1_M_CH2_DQS_13_DP	>>>	223	DM4/DQS13/TDQS13	DQ3	9	CPU1_M_CH2_DQ_03	(19,50)
(19,50) CPU1_M_CH2_DQS_12_DN	>>>	152	NC/DQS12_N/TDQS12_N	DQ2	4	CPU1_M_CH2_DQ_02	(19,50)
(19,50) CPU1_M_CH2_DQS_12_DP	>>>	151	DM3/DQS12/TDQS12	DQ1	3	CPU1_M_CH2_DQ_01	(19,50)
(19,50) CPU1_M_CH2_DQS_11_DN	>>>	144	NC/DQS11_N/TDQS11_N	DQ0	1	CPU1_M_CH2_DQ_00	(19,50)
(19,50) CPU1_M_CH2_DQS_11_DP	>>>	143	DM2/DQS11/TDQS11				
(19,50) CPU1_M_CH2_DQS_10_DN	>>>	135	NC/DQS10_N/TDQS10_N				
(19,50) CPU1_M_CH2_DQS_10_DP	>>>	134	DM1/DQS10/TDQS10				
(19,50) CPU1_M_CH2_DQS_09_DN	>>>	125	NC/DQS9_N/TDQS9_N				
(19,50) CPU1_M_CH2_DQS_09_DP	>>>	124	DM0/DQS9/TDQS9				
(19,50) CPU1_M_CH2_DQS_08_DN	>>>	42	DQS8_N				
(19,50) CPU1_M_CH2_DQS_08_DP	>>>	43	DQS8				
(19,50) CPU1_M_CH2_DQS_07_DN	>>>	111	DQS7_N				
(19,50) CPU1_M_CH2_DQS_07_DP	>>>	112	DQS7				
(19,50) CPU1_M_CH2_DQS_06_DN	>>>	103	DQS6_N				
(19,50) CPU1_M_CH2_DQS_06_DP	>>>	93	DQS6				
(19,50) CPU1_M_CH2_DQS_05_DN	>>>	94	DQS5_N				
(19,50) CPU1_M_CH2_DQS_05_DP	>>>	84	DQS5				
(19,50) CPU1_M_CH2_DQS_04_DN	>>>	85	DQS4_N				
(19,50) CPU1_M_CH2_DQS_04_DP	>>>	33	DQS4				
(19,50) CPU1_M_CH2_DQS_03_DN	>>>	24	DQS3_N				
(19,50) CPU1_M_CH2_DQS_03_DP	>>>	25	DQS3				
(19,50) CPU1_M_CH2_DQS_02_DN	>>>	15	DQS2_N				
(19,50) CPU1_M_CH2_DQS_02_DP	>>>	16	DQS2				
(19,50) CPU1_M_CH2_DQS_01_DN	>>>	6	DQS1_N				
(19,50) CPU1_M_CH2_DQS_01_DP	>>>	7	DQS1				
(19,50) CPU1_M_CH2_DQS_00_DN	>>>	53	DQS0_N				
(19,50) CPU1_M_CH2_DQS_00_DP	>>>	68	DQS0				
(19,50) CPU1_M_CH2_PERR_N	>>>	167	ERR_OUT_N/NC				
(19,50) CPU1_M_CH2_MA_PAR	>>>	167	PAR_IN/NC				
(19,50) CPU1_M_CH2_MA_PAR	>>>	167	NC/TEST				

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SPD = 0xA2
TSOD = 0x32

EVENT_N/NC
RESET_N

DIMM_TEMP_EVENT_N (47,48,50,53,54,60,61,63,64,66,67,153)
CPU1_M_CH23_RST_N (16,50,53,54)

2	VSS_2	124	124
5	VSS_5	VSS_127	127
8	VSS_8	VSS_130	130
11	VSS_11	VSS_133	133
14	VSS_14	VSS_136	136
17	VSS_17	VSS_139	139
20	VSS_20	VSS_142	142
23	VSS_23	VSS_145	145
26	VSS_26	VSS_148	148
29	VSS_29	VSS_151	151
32	VSS_32	VSS_154	154
35	VSS_35	VSS_157	157
38	VSS_38	VSS_160	160
41	VSS_41	VSS_163	163
44	VSS_44	VSS_166	166
47	VSS_47	VSS_169	169
50	VSS_50	VSS_172	172
53	VSS_53	VSS_175	175
56	VSS_56	VSS_178	178
59	VSS_59	VSS_181	181
62	VSS_62	VSS_184	184
65	VSS_65	VSS_187	187
68	VSS_68	VSS_190	190
71	VSS_71	VSS_193	193
74	VSS_74	VSS_196	196
77	VSS_77	VSS_199	199
80	VSS_80	VSS_202	202
83	VSS_83	VSS_205	205
86	VSS_86	VSS_208	208
89	VSS_89	VSS_211	211
92	VSS_92	VSS_214	214
95	VSS_95	VSS_217	217
98	VSS_98	VSS_220	220
101	VSS_101	VSS_223	223
104	VSS_104	VSS_226	226
107	VSS_107	VSS_229	229
110	VSS_110	VSS_232	232
113	VSS_113	VSS_235	235
116	VSS_116	VSS_238	238
119	VSS_119	VSS_241	241
122	VSS_122	VSS_244	244

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V_MEM_VTT_CPU1

C561
10uF
+/-20%
C0603H0_9
X5R
6.3V

C567
10uF
+/-20%
C0603H0_9
X5R
6.3V

Harbor City use 0805 47uF x5.

C493
10uF
+/-20%
C0603H0_9
X5R
6.3V

C458
10uF
+/-20%
C0603H0_9
X5R
6.3V

C483
10uF
+/-20%
C0603H0_9
X5R
6.3V

C465
10uF
+/-20%
C0603H0_9
X5R
6.3V

C479
10uF
+/-20%
C0603H0_9
X5R
6.3V

C451
10uF
+/-20%
C0603H0_9
X5R
6.3V

C446
10uF
+/-20%
C0603H0_9
X5R
6.3V

C501
10uF
+/-20%
C0603H0_9
X5R
6.3V

FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)
Hon Hai Precision Ind. Co., Ltd.

Title
CPU1 CH2 DIMM1

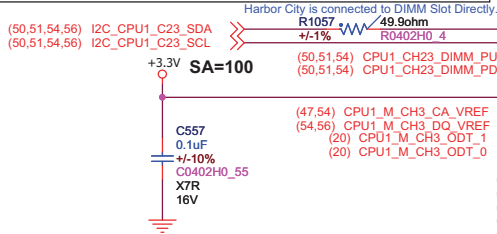
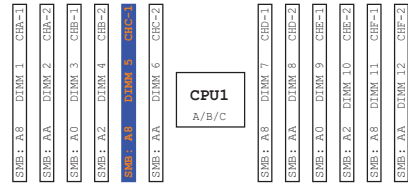
Document Number:
PCB P/N: 01015C800-000-G

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DIMM population

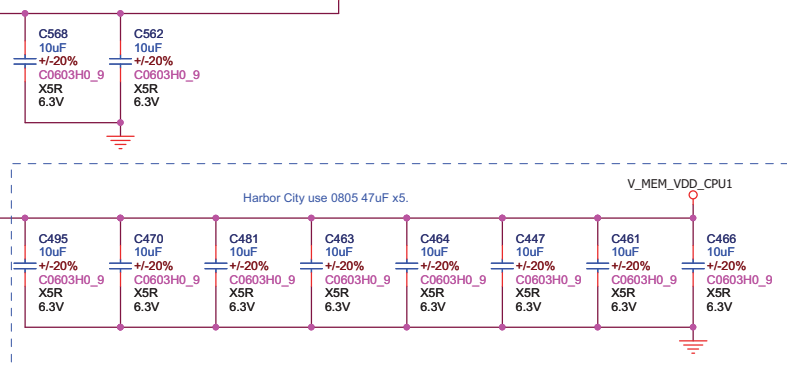
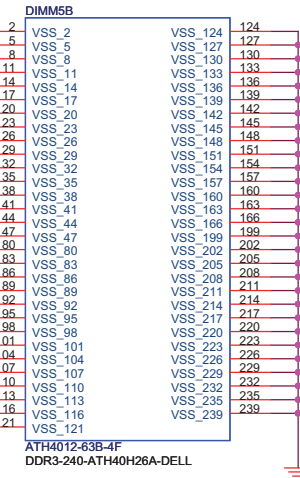


(20,54) CPU1_M_CH3_BA_2	52	B2	DO63	234	CPU1_M_CH3_DQ_63	(20,54)
(20,54) CPU1_M_CH3_BA_1	190	BA1	DO62	233	CPU1_M_CH3_DQ_62	(20,54)
(20,54) CPU1_M_CH3_BA_0	71	BA0	DO61	228	CPU1_M_CH3_DQ_61	(20,54)
(20,54) CPU1_M_CH3_MA_15	171	A15/NC	DO60	227	CPU1_M_CH3_DQ_60	(20,54)
(20,54) CPU1_M_CH3_MA_14	172	A14	DO59	114	CPU1_M_CH3_DQ_59	(20,54)
(20,54) CPU1_M_CH3_MA_13	173	A13	DO58	109	CPU1_M_CH3_DQ_58	(20,54)
(20,54) CPU1_M_CH3_MA_12	174	A12_BC_N	DO57	108	CPU1_M_CH3_DQ_57	(20,54)
(20,54) CPU1_M_CH3_MA_11	55	A11	DO56	225	CPU1_M_CH3_DQ_56	(20,54)
(20,54) CPU1_M_CH3_MA_10	70	A10/AP	DO55	224	CPU1_M_CH3_DQ_55	(20,54)
(20,54) CPU1_M_CH3_MA_09	175	A9	DO54	224	CPU1_M_CH3_DQ_54	(20,54)
(20,54) CPU1_M_CH3_MA_08	177	A8	DO53	219	CPU1_M_CH3_DQ_53	(20,54)
(20,54) CPU1_M_CH3_MA_07	56	A7	DO52	218	CPU1_M_CH3_DQ_52	(20,54)
(20,54) CPU1_M_CH3_MA_06	178	A6	DO51	105	CPU1_M_CH3_DQ_51	(20,54)
(20,54) CPU1_M_CH3_MA_05	58	A5	DO50	100	CPU1_M_CH3_DQ_50	(20,54)
(20,54) CPU1_M_CH3_MA_04	59	A4	DO49	99	CPU1_M_CH3_DQ_49	(20,54)
(20,54) CPU1_M_CH3_MA_03	180	A3	DO48	99	CPU1_M_CH3_DQ_48	(20,54)
(20,54) CPU1_M_CH3_MA_02	61	A2	DO47	216	CPU1_M_CH3_DQ_47	(20,54)
(20,54) CPU1_M_CH3_MA_01	181	A1	DO46	215	CPU1_M_CH3_DQ_46	(20,54)
(20,54) CPU1_M_CH3_MA_00	188	A0	DO45	210	CPU1_M_CH3_DQ_45	(20,54)
(20) CPU1_M_CH3_CS_3_N	198	S3_N/NC	DO44	97	CPU1_M_CH3_DQ_44	(20,54)
(20) CPU1_M_CH3_CS_2_N	79	S2_N/NC	DO43	96	CPU1_M_CH3_DQ_43	(20,54)
(20) CPU1_M_CH3_CS_1_N	76	S1_N/NC	DO42	91	CPU1_M_CH3_DQ_42	(20,54)
(20) CPU1_M_CH3_CS_0_N	193	S0_N	DO41	90	CPU1_M_CH3_DQ_41	(20,54)
(20,54) CPU1_M_CH3_RAS_N	192	RAS_N	DO39	207	CPU1_M_CH3_DQ_39	(20,54)
(20,54) CPU1_M_CH3_CAS_N	74	CAS_N	DO38	201	CPU1_M_CH3_DQ_38	(20,54)
(20,54) CPU1_M_CH3_WE_N	63	WE_N	DO37	200	CPU1_M_CH3_DQ_37	(20,54)
(20) CPU1_M_CH3_CK_2_DP	64	CK_2	DO36	88	CPU1_M_CH3_DQ_36	(20,54)
(20) CPU1_M_CH3_CK_2_DN	185	CK_2	DO35	87	CPU1_M_CH3_DQ_35	(20,54)
(20) CPU1_M_CH3_CK_0_DP	184	CK_0	DO34	82	CPU1_M_CH3_DQ_34	(20,54)
(20) CPU1_M_CH3_CK_0_DN	169	CK_0	DO33	81	CPU1_M_CH3_DQ_33	(20,54)
(20) CPU1_M_CH3_CKE_1	50	CKE1/NC	DO32	156	CPU1_M_CH3_DQ_32	(20,54)
(20) CPU1_M_CH3_CKE_0	50	CKE0	DO31	155	CPU1_M_CH3_DQ_31	(20,54)
	238	SDA	DO30	150	CPU1_M_CH3_DQ_30	(20,54)
	118	SCL	DO29	149	CPU1_M_CH3_DQ_29	(20,54)
	119	SA2	DO28	37	CPU1_M_CH3_DQ_28	(20,54)
	237	SA1	DO27	36	CPU1_M_CH3_DQ_27	(20,54)
	117	SA0	DO26	31	CPU1_M_CH3_DQ_26	(20,54)
	236	VDDSPD	DO25	30	CPU1_M_CH3_DQ_25	(20,54)
	67	VREFCA	DO24	147	CPU1_M_CH3_DQ_24	(20,54)
	1	VREFDQ	DO23	141	CPU1_M_CH3_DQ_23	(20,54)
	195	ODT1/NC	DO22	141	CPU1_M_CH3_DQ_22	(20,54)
	165	ODT0	DO21	140	CPU1_M_CH3_DQ_21	(20,54)
(20,54) CPU1_M_CH3_ECC_7	165	CB7/NC	DO19	28	CPU1_M_CH3_DQ_19	(20,54)
(20,54) CPU1_M_CH3_ECC_6	164	CB6/NC	DO18	27	CPU1_M_CH3_DQ_18	(20,54)
(20,54) CPU1_M_CH3_ECC_5	158	CB5/NC	DO17	22	CPU1_M_CH3_DQ_17	(20,54)
(20,54) CPU1_M_CH3_ECC_4	158	CB4/NC	DO16	138	CPU1_M_CH3_DQ_16	(20,54)
(20,54) CPU1_M_CH3_ECC_3	45	CB3/NC	DO15	137	CPU1_M_CH3_DQ_15	(20,54)
(20,54) CPU1_M_CH3_ECC_2	45	CB2/NC	DO14	132	CPU1_M_CH3_DQ_14	(20,54)
(20,54) CPU1_M_CH3_ECC_1	40	CB1/NC	DO13	131	CPU1_M_CH3_DQ_13	(20,54)
(20,54) CPU1_M_CH3_ECC_0	39	CB0/NC	DO12	19	CPU1_M_CH3_DQ_12	(20,54)
	162	NC/DQS17_N/TDQS17_N	DO11	18	CPU1_M_CH3_DQ_11	(20,54)
(20,54) CPU1_M_CH3_DQS_17_DN	161	DM8/DQS17/TDQS17/NC	DO10	13	CPU1_M_CH3_DQ_10	(20,54)
(20,54) CPU1_M_CH3_DQS_16_DN	231	NC/DQS16_N/TDQS16_N	DO9	12	CPU1_M_CH3_DQ_09	(20,54)
(20,54) CPU1_M_CH3_DQS_16_DP	230	DM7/DQS16/TDQS16	DO8	129	CPU1_M_CH3_DQ_08	(20,54)
(20,54) CPU1_M_CH3_DQS_15_DN	222	NC/DQS15_N/TDQS15_N	DO7	128	CPU1_M_CH3_DQ_07	(20,54)
(20,54) CPU1_M_CH3_DQS_15_DP	221	DM6/DQS15/TDQS15	DO6	123	CPU1_M_CH3_DQ_06	(20,54)
(20,54) CPU1_M_CH3_DQS_14_DN	213	NC/DQS14_N/TDQS14_N	DO5	122	CPU1_M_CH3_DQ_05	(20,54)
(20,54) CPU1_M_CH3_DQS_14_DP	212	DM5/DQS14/TDQS14	DO4	10	CPU1_M_CH3_DQ_04	(20,54)
(20,54) CPU1_M_CH3_DQS_13_DN	204	NC/DQS13_N/TDQS13_N	DO3	9	CPU1_M_CH3_DQ_03	(20,54)
(20,54) CPU1_M_CH3_DQS_13_DP	203	DM4/DQS13/TDQS13	DO2	4	CPU1_M_CH3_DQ_02	(20,54)
(20,54) CPU1_M_CH3_DQS_12_DN	153	NC/DQS12_N/TDQS12_N	DO1	4	CPU1_M_CH3_DQ_01	(20,54)
(20,54) CPU1_M_CH3_DQS_12_DP	152	DM3/DQS12/TDQS12	DO0	3	CPU1_M_CH3_DQ_00	(20,54)
(20,54) CPU1_M_CH3_DQS_11_DN	144	NC/DQS11_N/TDQS11_N				
(20,54) CPU1_M_CH3_DQS_11_DP	143	DM2/DQS11/TDQS11				
(20,54) CPU1_M_CH3_DQS_10_DN	135	NC/DQS10_N/TDQS10_N				
(20,54) CPU1_M_CH3_DQS_10_DP	134	DM1/DQS10/TDQS10				
(20,54) CPU1_M_CH3_DQS_09_DN	126	NC/DQS9_N/TDQS9_N				
(20,54) CPU1_M_CH3_DQS_09_DP	125	DM0/DQS9/TDQS9				
(20,54) CPU1_M_CH3_DQS_08_DN	42	DQS8_N				
(20,54) CPU1_M_CH3_DQS_08_DP	43	DQS8				
(20,54) CPU1_M_CH3_DQS_07_DN	111	DQS7_N				
(20,54) CPU1_M_CH3_DQS_07_DP	112	DQS7				
(20,54) CPU1_M_CH3_DQS_06_DN	103	DQS6_N				
(20,54) CPU1_M_CH3_DQS_06_DP	93	DQS6				
(20,54) CPU1_M_CH3_DQS_05_DN	94	DQS5_N				
(20,54) CPU1_M_CH3_DQS_05_DP	84	DQS5				
(20,54) CPU1_M_CH3_DQS_04_DN	85	DQS4_N				
(20,54) CPU1_M_CH3_DQS_04_DP	33	DQS4				
(20,54) CPU1_M_CH3_DQS_03_DN	24	DQS3_N				
(20,54) CPU1_M_CH3_DQS_03_DP	25	DQS3				
(20,54) CPU1_M_CH3_DQS_02_DN	15	DQS2_N				
(20,54) CPU1_M_CH3_DQS_02_DP	16	DQS2				
(20,54) CPU1_M_CH3_DQS_01_DN	6	DQS1_N				
(20,54) CPU1_M_CH3_DQS_01_DP	7	DQS1				
(20,54) CPU1_M_CH3_DQS_00_DN	53	DQS0_N				
(20,54) CPU1_M_CH3_DQS_00_DP	68	DQS0				
(20,54) CPU1_M_CH3_PERR_N	167	ERR_OUT_N/NC				
(20,54) CPU1_M_CH3_MA_PAR		PAR_IN/NC				
		NC/TEST				

ATH4012-638-4F
DDR3-240-ATH40H26A-DELL

SPD = 0xA8
TSOD = 0x38

EVENT_N/NC
RESET_N
DIMM_TEMP_EVENT_N (47,48,50,51,54,60,61,63,64,66,67,153)
CPU1_M_CH23_RST_N (16,50,51,54)



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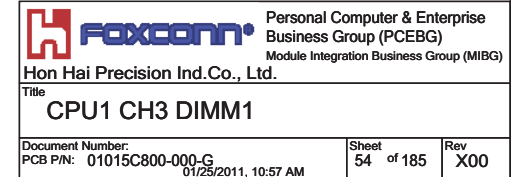
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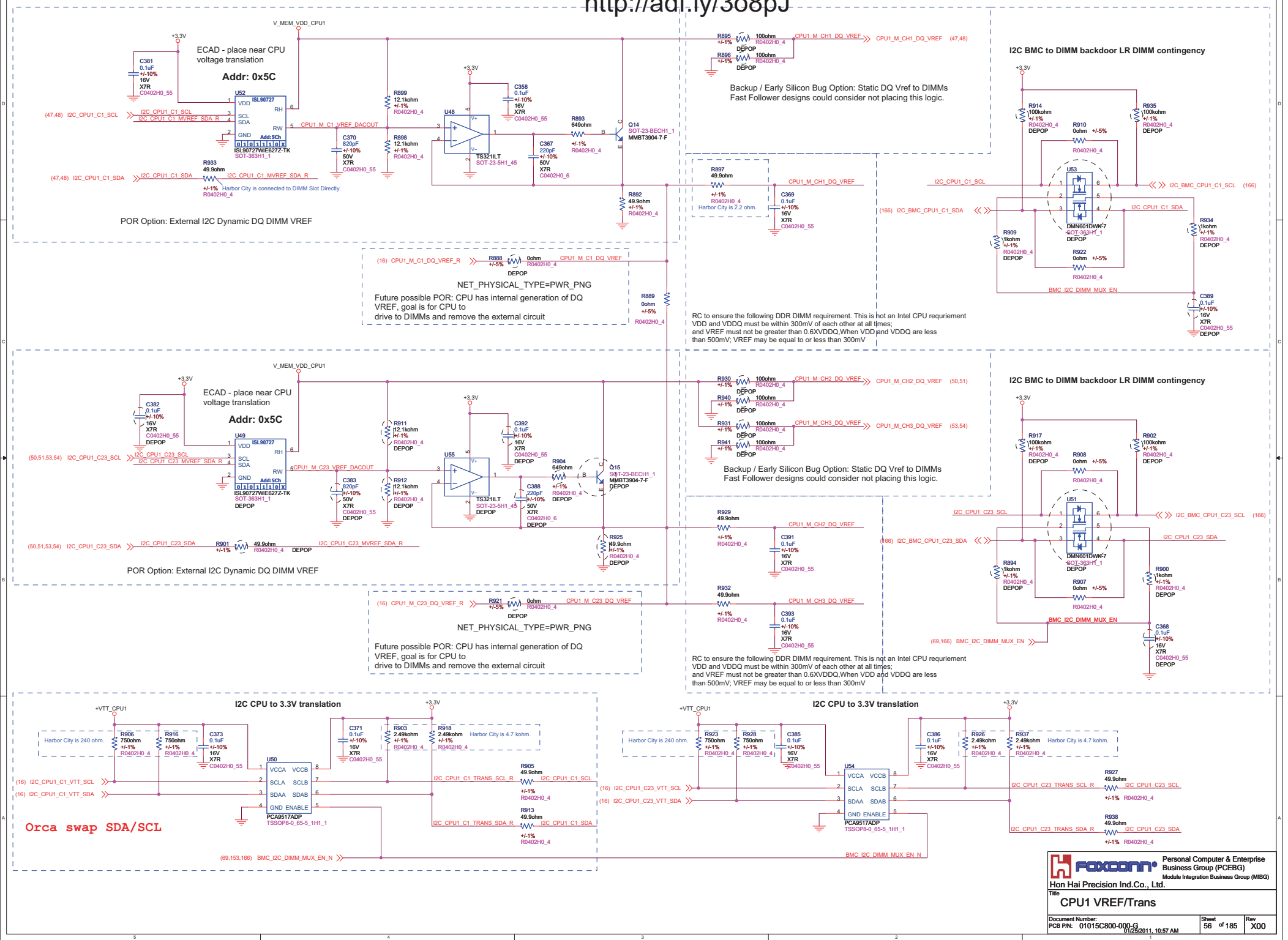
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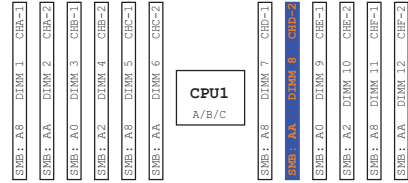
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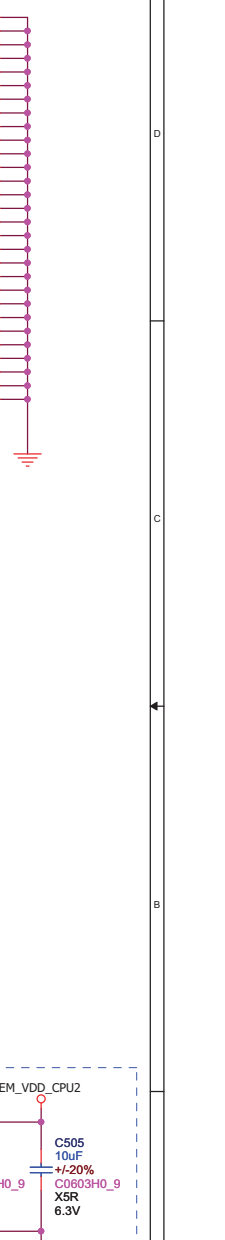
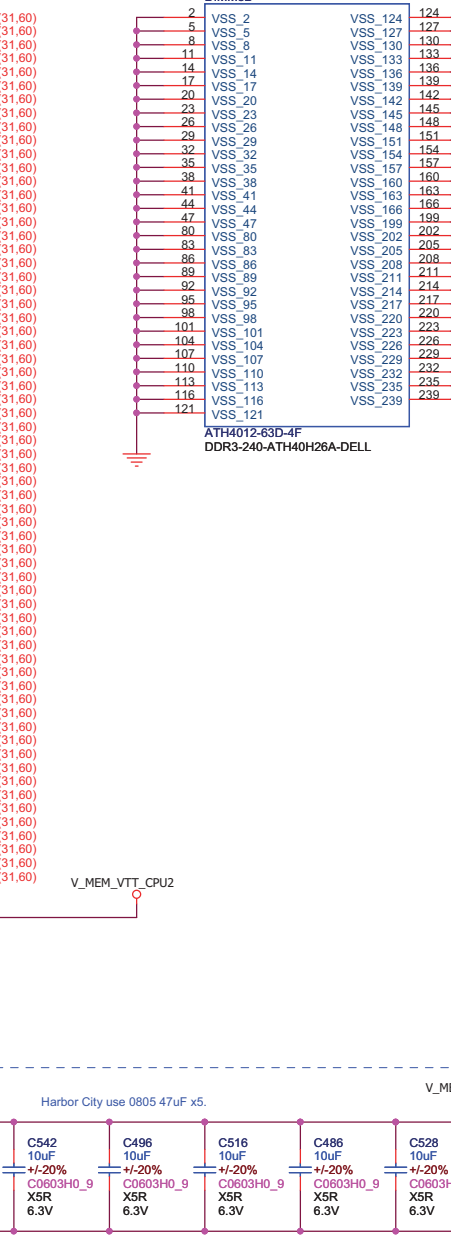


DIMM population



(31,60) CPU2_M.CH1.BA_2	52	BA2
(31,60) CPU2_M.CH1.BA_1	190	BA1
(31,60) CPU2_M.CH1.BA_0	71	BA0
(31,60) CPU2_M.CH1.MA_15	171	A15/NC
(31,60) CPU2_M.CH1.MA_14	172	A14
(31,60) CPU2_M.CH1.MA_13	198	A13
(31,60) CPU2_M.CH1.MA_12	174	A12_BC_N
(31,60) CPU2_M.CH1.MA_11	55	A11
(31,60) CPU2_M.CH1.MA_10	70	A10/AP
(31,60) CPU2_M.CH1.MA_09	175	A9
(31,60) CPU2_M.CH1.MA_08	177	A8
(31,60) CPU2_M.CH1.MA_07	56	A7
(31,60) CPU2_M.CH1.MA_06	178	A6
(31,60) CPU2_M.CH1.MA_05	58	A5
(31,60) CPU2_M.CH1.MA_04	59	A4
(31,60) CPU2_M.CH1.MA_03	180	A3
(31,60) CPU2_M.CH1.MA_02	61	A2
(31,60) CPU2_M.CH1.MA_01	181	A1
(31,60) CPU2_M.CH1.MA_00	188	A0
(31) CPU2_M.CH1_CS_7_N	198	S3_N/NC
(31) CPU2_M.CH1_CS_6_N	79	S2_N/NC
(31) CPU2_M.CH1_CS_5_N	76	S1_N/NC
(31) CPU2_M.CH1_CS_4_N	193	S0_N
(31,60) CPU2_M.CH1.RAS_N	192	RAS_N
(31,60) CPU2_M.CH1.CAS_N	74	CAS_N
(31,60) CPU2_M.CH1.WE_N	63	WE_N
(31) CPU2_M.CH1.CK_3_DP	64	NC_CK1_N
(31) CPU2_M.CH1.CK_3_N	185	CK1_N
(31) CPU2_M.CH1.CK_1_DP	184	CK0_N
(31) CPU2_M.CH1.CK_1_N	169	CKE1/NC
(31) CPU2_M.CH1.CKE_2	50	CKE0
(31) CPU2_M.CH1.CKE_1	238	SDA
(31) CPU2_M.CH1.CKE_0	118	SCL
(60,69) I2C_CPU2_C1_SDA	119	SA2
(60,69) I2C_CPU2_C1_SCL	237	SA1
(60) CPU2_CH1_DIMM_PU	117	SA0
(60) CPU2_CH1_DIMM_PD	236	VDDSPD
(60) CPU2_M.CH1_CA_VREF	67	VREFCA
(60,69) CPU2_M.CH1_DQ_VREF	1	VREFDQ
(31) CPU2_M.CH1_ODT_3	77	ODT1/NC
(31) CPU2_M.CH1_ODT_2	195	ODT0
(31,60) CPU2_M.CH1.ECC_7	165	CB7/NC
(31,60) CPU2_M.CH1.ECC_6	164	CB6/NC
(31,60) CPU2_M.CH1.ECC_5	159	CB5/NC
(31,60) CPU2_M.CH1.ECC_4	158	CB4/NC
(31,60) CPU2_M.CH1.ECC_3	46	CB3/NC
(31,60) CPU2_M.CH1.ECC_2	45	CB2/NC
(31,60) CPU2_M.CH1.ECC_1	40	CB1/NC
(31,60) CPU2_M.CH1.ECC_0	39	CB0/NC
(31,60) CPU2_M.CH1.DQS_17_DN	162	NC/DQS17_N/TDQS17_N
(31,60) CPU2_M.CH1.DQS_17_DP	161	DM8/DQS17/TDQS17/NC
(31,60) CPU2_M.CH1.DQS_16_DN	231	NC/DQS16_N/TDQS16_N
(31,60) CPU2_M.CH1.DQS_16_DP	230	DM7/DQS16/TDQS16/NC
(31,60) CPU2_M.CH1.DQS_15_DN	222	NC/DQS15_N/TDQS15_N
(31,60) CPU2_M.CH1.DQS_15_DP	221	DM6/DQS15/TDQS15/NC
(31,60) CPU2_M.CH1.DQS_14_DN	213	NC/DQS14_N/TDQS14_N
(31,60) CPU2_M.CH1.DQS_14_DP	212	DM5/DQS14/TDQS14/NC
(31,60) CPU2_M.CH1.DQS_13_DN	204	NC/DQS13_N/TDQS13_N
(31,60) CPU2_M.CH1.DQS_13_DP	203	DM4/DQS13/TDQS13/NC
(31,60) CPU2_M.CH1.DQS_12_DN	153	NC/DQS12_N/TDQS12_N
(31,60) CPU2_M.CH1.DQS_12_DP	152	DM3/DQS12/TDQS12/NC
(31,60) CPU2_M.CH1.DQS_11_DN	144	NC/DQS11_N/TDQS11_N
(31,60) CPU2_M.CH1.DQS_11_DP	143	DM2/DQS11/TDQS11/NC
(31,60) CPU2_M.CH1.DQS_10_DN	135	NC/DQS10_N/TDQS10_N
(31,60) CPU2_M.CH1.DQS_10_DP	134	DM1/DQS10/TDQS10/NC
(31,60) CPU2_M.CH1.DQS_09_DN	126	NC/DQS9_N/TDQS9_N
(31,60) CPU2_M.CH1.DQS_09_DP	125	DM0/DQS9/TDQS9/NC
(31,60) CPU2_M.CH1.DQS_08_DN	42	DQS8_N
(31,60) CPU2_M.CH1.DQS_08_DP	43	DQS8_N
(31,60) CPU2_M.CH1.DQS_07_DN	111	DQS7_N
(31,60) CPU2_M.CH1.DQS_07_DP	112	DQS7_N
(31,60) CPU2_M.CH1.DQS_06_DN	102	DQS6_N
(31,60) CPU2_M.CH1.DQS_06_DP	103	DQS6_N
(31,60) CPU2_M.CH1.DQS_05_DN	93	DQS5_N
(31,60) CPU2_M.CH1.DQS_05_DP	94	DQS5_N
(31,60) CPU2_M.CH1.DQS_04_DN	84	DQS4_N
(31,60) CPU2_M.CH1.DQS_04_DP	85	DQS4_N
(31,60) CPU2_M.CH1.DQS_03_DN	33	DQS3_N
(31,60) CPU2_M.CH1.DQS_03_DP	34	DQS3_N
(31,60) CPU2_M.CH1.DQS_02_DN	24	DQS2_N
(31,60) CPU2_M.CH1.DQS_02_DP	25	DQS2_N
(31,60) CPU2_M.CH1.DQS_01_DN	15	DQS1_N
(31,60) CPU2_M.CH1.DQS_01_DP	16	DQS1_N
(31,60) CPU2_M.CH1.DQS_00_DN	6	DQS0_N
(31,60) CPU2_M.CH1.DQS_00_DP	7	DQS0_N
(31,60) CPU2_M.CH1.PERR_N	53	ERR_OUT_N/NC
(31,60) CPU2_M.CH1.MA_PAR	68	PAR_IN/NC
(31,60) CPU2_M.CH1.MA_PAR	167	NC/TEST

DO63	234	CPU2_M.CH1.DQ_63 (31,60)
DO62	233	CPU2_M.CH1.DQ_62 (31,60)
DO61	228	CPU2_M.CH1.DQ_61 (31,60)
DO60	227	CPU2_M.CH1.DQ_60 (31,60)
DO59	114	CPU2_M.CH1.DQ_59 (31,60)
DO58	109	CPU2_M.CH1.DQ_58 (31,60)
DO57	108	CPU2_M.CH1.DQ_57 (31,60)
DO56	225	CPU2_M.CH1.DQ_56 (31,60)
DO55	224	CPU2_M.CH1.DQ_55 (31,60)
DO54	225	CPU2_M.CH1.DQ_54 (31,60)
DO53	219	CPU2_M.CH1.DQ_53 (31,60)
DO52	218	CPU2_M.CH1.DQ_52 (31,60)
DO51	105	CPU2_M.CH1.DQ_51 (31,60)
DO50	100	CPU2_M.CH1.DQ_50 (31,60)
DO49	99	CPU2_M.CH1.DQ_49 (31,60)
DO48	216	CPU2_M.CH1.DQ_48 (31,60)
DO47	215	CPU2_M.CH1.DQ_47 (31,60)
DO46	215	CPU2_M.CH1.DQ_46 (31,60)
DO45	210	CPU2_M.CH1.DQ_45 (31,60)
DO44	209	CPU2_M.CH1.DQ_44 (31,60)
DO43	96	CPU2_M.CH1.DQ_43 (31,60)
DO42	95	CPU2_M.CH1.DQ_42 (31,60)
DO41	91	CPU2_M.CH1.DQ_41 (31,60)
DO40	90	CPU2_M.CH1.DQ_40 (31,60)
DO39	207	CPU2_M.CH1.DQ_39 (31,60)
DO38	206	CPU2_M.CH1.DQ_38 (31,60)
DO37	201	CPU2_M.CH1.DQ_37 (31,60)
DO36	88	CPU2_M.CH1.DQ_36 (31,60)
DO35	87	CPU2_M.CH1.DQ_35 (31,60)
DO34	82	CPU2_M.CH1.DQ_34 (31,60)
DO33	82	CPU2_M.CH1.DQ_33 (31,60)
DO32	81	CPU2_M.CH1.DQ_32 (31,60)
DO31	156	CPU2_M.CH1.DQ_31 (31,60)
DO30	155	CPU2_M.CH1.DQ_30 (31,60)
DO29	149	CPU2_M.CH1.DQ_29 (31,60)
DO28	37	CPU2_M.CH1.DQ_28 (31,60)
DO27	36	CPU2_M.CH1.DQ_27 (31,60)
DO26	31	CPU2_M.CH1.DQ_26 (31,60)
DO25	30	CPU2_M.CH1.DQ_25 (31,60)
DO24	30	CPU2_M.CH1.DQ_24 (31,60)
DO23	147	CPU2_M.CH1.DQ_23 (31,60)
DO22	141	CPU2_M.CH1.DQ_22 (31,60)
DO21	140	CPU2_M.CH1.DQ_21 (31,60)
DO20	28	CPU2_M.CH1.DQ_20 (31,60)
DO19	27	CPU2_M.CH1.DQ_19 (31,60)
DO18	27	CPU2_M.CH1.DQ_18 (31,60)
DO17	22	CPU2_M.CH1.DQ_17 (31,60)
DO16	21	CPU2_M.CH1.DQ_16 (31,60)
DO15	138	CPU2_M.CH1.DQ_15 (31,60)
DO14	137	CPU2_M.CH1.DQ_14 (31,60)
DO13	132	CPU2_M.CH1.DQ_13 (31,60)
DO12	131	CPU2_M.CH1.DQ_12 (31,60)
DO11	19	CPU2_M.CH1.DQ_11 (31,60)
DO10	18	CPU2_M.CH1.DQ_10 (31,60)
DO9	13	CPU2_M.CH1.DQ_09 (31,60)
DO8	12	CPU2_M.CH1.DQ_08 (31,60)
DO7	129	CPU2_M.CH1.DQ_07 (31,60)
DO6	128	CPU2_M.CH1.DQ_06 (31,60)
DO5	123	CPU2_M.CH1.DQ_05 (31,60)
DO4	122	CPU2_M.CH1.DQ_04 (31,60)
DO3	10	CPU2_M.CH1.DQ_03 (31,60)
DO2	9	CPU2_M.CH1.DQ_02 (31,60)
DO1	4	CPU2_M.CH1.DQ_01 (31,60)
DO0	3	CPU2_M.CH1.DQ_00 (31,60)



SPD = 0xAA
TSOD = 0x3A

FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)

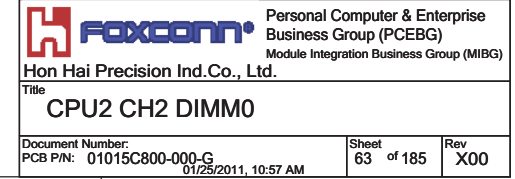
Hon Hai Precision Ind. Co., Ltd.

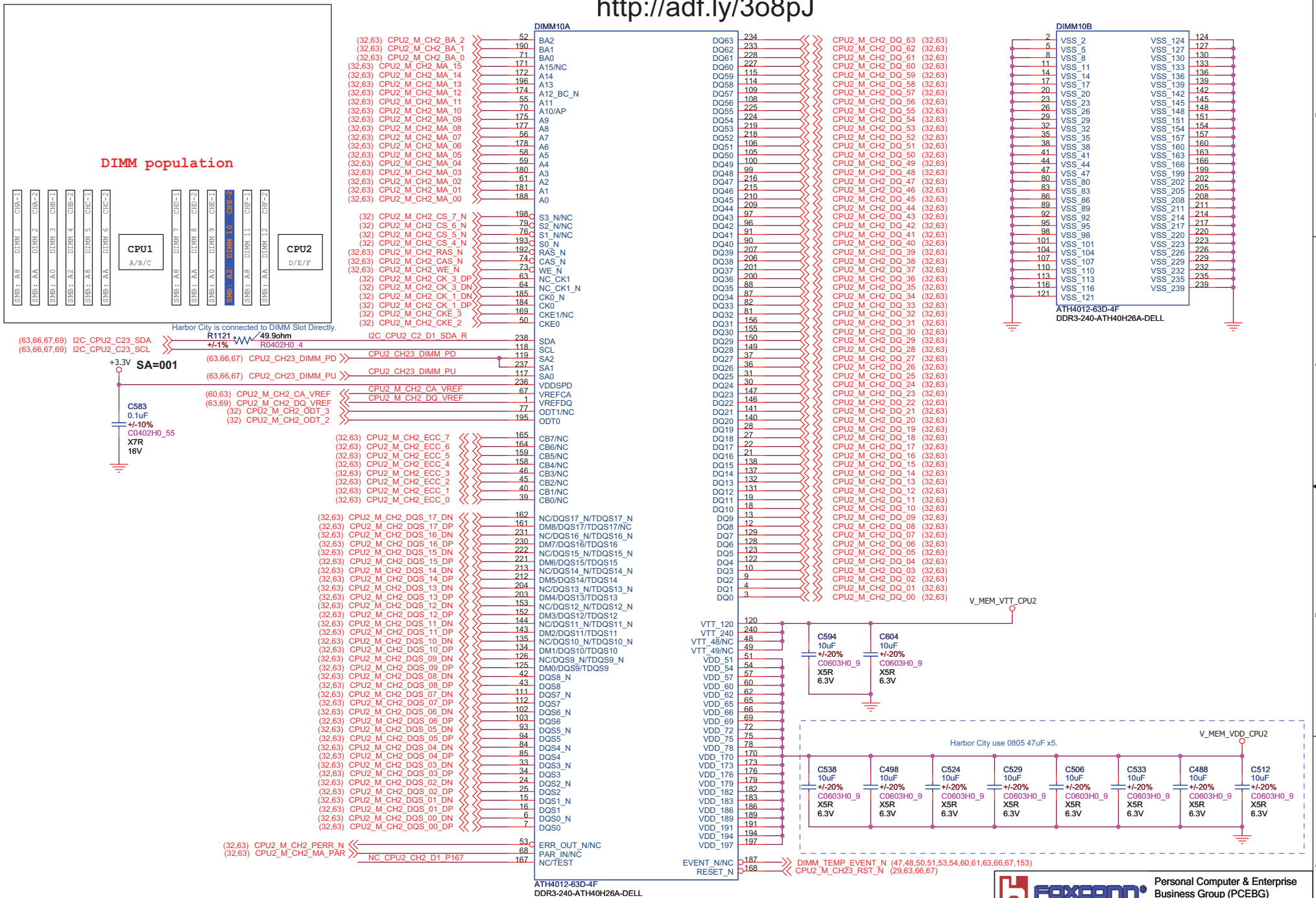
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Document Number: 01015C800-000-G
PCB P/N: 01015C800-000-G

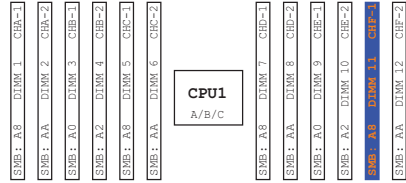
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DIMM population



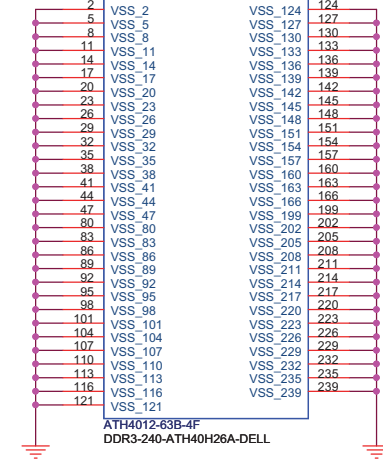
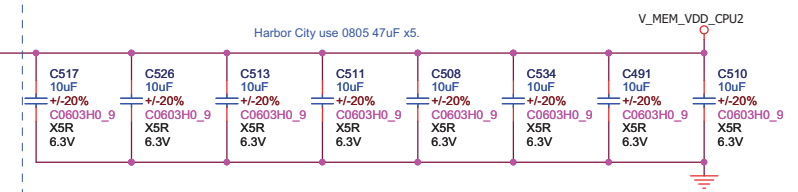
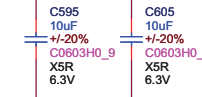
(33,67) CPU2_M_CH3_BA_2	52	BA2
(33,67) CPU2_M_CH3_BA_1	190	BA1
(33,67) CPU2_M_CH3_BA_0	71	BA0
(33,67) CPU2_M_CH3_MA_15	171	A15/NC
(33,67) CPU2_M_CH3_MA_14	172	A14
(33,67) CPU2_M_CH3_MA_13	198	A13
(33,67) CPU2_M_CH3_MA_12	174	A12_BC_N
(33,67) CPU2_M_CH3_MA_11	55	A11
(33,67) CPU2_M_CH3_MA_10	70	A10/AP
(33,67) CPU2_M_CH3_MA_09	175	A9
(33,67) CPU2_M_CH3_MA_08	177	A8
(33,67) CPU2_M_CH3_MA_07	56	A7
(33,67) CPU2_M_CH3_MA_06	178	A6
(33,67) CPU2_M_CH3_MA_05	58	A5
(33,67) CPU2_M_CH3_MA_04	59	A4
(33,67) CPU2_M_CH3_MA_03	180	A3
(33,67) CPU2_M_CH3_MA_02	61	A2
(33,67) CPU2_M_CH3_MA_01	181	A1
(33,67) CPU2_M_CH3_MA_00	188	A0
(33) CPU2_M_CH3_CS_3_N	198	S3_N/NC
(33) CPU2_M_CH3_CS_2_N	79	S2_N/NC
(33) CPU2_M_CH3_CS_1_N	76	S1_N/NC
(33) CPU2_M_CH3_CS_0_N	193	S0_N
(33,67) CPU2_M_CH3_RAS_N	192	RAS_N
(33,67) CPU2_M_CH3_CAS_N	74	CAS_N
(33,67) CPU2_M_CH3_WE_N	63	WE_N
(33) CPU2_M_CH3_CK_2_DP	64	NC_CK1_N
(33) CPU2_M_CH3_CK_2_DN	185	CK0_N
(33) CPU2_M_CH3_CK_0_DP	184	CK0
(33) CPU2_M_CH3_CK_0_DN	169	CKE1/NC
(33) CPU2_M_CH3_CKE_1	50	CKE0
(33) CPU2_M_CH3_CKE_0	50	CKE0
(33,67) CPU2_M_CH3_ECC_7	165	CB7/NC
(33,67) CPU2_M_CH3_ECC_6	164	CB6/NC
(33,67) CPU2_M_CH3_ECC_5	159	CB5/NC
(33,67) CPU2_M_CH3_ECC_4	158	CB4/NC
(33,67) CPU2_M_CH3_ECC_3	46	CB3/NC
(33,67) CPU2_M_CH3_ECC_2	45	CB2/NC
(33,67) CPU2_M_CH3_ECC_1	40	CB1/NC
(33,67) CPU2_M_CH3_ECC_0	39	CB0/NC
(33,67) CPU2_M_CH3_DQS_17_DN	162	NC/DQS17_N/TDQS17_N
(33,67) CPU2_M_CH3_DQS_17_DP	161	DM8/DQS17/TDQS17/NC
(33,67) CPU2_M_CH3_DQS_16_DN	231	NC/DQS16_N/TDQS16_N
(33,67) CPU2_M_CH3_DQS_16_DP	230	DM7/DQS16/TDQS16/NC
(33,67) CPU2_M_CH3_DQS_15_DN	222	NC/DQS15_N/TDQS15_N
(33,67) CPU2_M_CH3_DQS_15_DP	221	DM6/DQS15/TDQS15
(33,67) CPU2_M_CH3_DQS_14_DN	213	NC/DQS14_N/TDQS14_N
(33,67) CPU2_M_CH3_DQS_14_DP	212	DM5/DQS14/TDQS14
(33,67) CPU2_M_CH3_DQS_13_DN	204	NC/DQS13_N/TDQS13_N
(33,67) CPU2_M_CH3_DQS_13_DP	203	DM4/DQS13/TDQS13
(33,67) CPU2_M_CH3_DQS_12_DN	153	NC/DQS12_N/TDQS12_N
(33,67) CPU2_M_CH3_DQS_12_DP	152	DM3/DQS12/TDQS12
(33,67) CPU2_M_CH3_DQS_11_DN	144	NC/DQS11_N/TDQS11_N
(33,67) CPU2_M_CH3_DQS_11_DP	143	DM2/DQS11/TDQS11
(33,67) CPU2_M_CH3_DQS_10_DN	135	NC/DQS10_N/TDQS10_N
(33,67) CPU2_M_CH3_DQS_10_DP	134	DM1/DQS10/TDQS10
(33,67) CPU2_M_CH3_DQS_09_DN	125	NC/DQS9_N/TDQS9_N
(33,67) CPU2_M_CH3_DQS_09_DP	124	DM0/DQS9/TDQS9
(33,67) CPU2_M_CH3_DQS_08_DN	42	DQS8_N
(33,67) CPU2_M_CH3_DQS_08_DP	43	DQS8
(33,67) CPU2_M_CH3_DQS_07_DN	111	DQS7_N
(33,67) CPU2_M_CH3_DQS_07_DP	112	DQS7
(33,67) CPU2_M_CH3_DQS_06_DN	102	DQS6_N
(33,67) CPU2_M_CH3_DQS_06_DP	103	DQS6
(33,67) CPU2_M_CH3_DQS_05_DN	93	DQS5_N
(33,67) CPU2_M_CH3_DQS_05_DP	94	DQS5
(33,67) CPU2_M_CH3_DQS_04_DN	84	DQS4_N
(33,67) CPU2_M_CH3_DQS_04_DP	85	DQS4
(33,67) CPU2_M_CH3_DQS_03_DN	33	DQS3_N
(33,67) CPU2_M_CH3_DQS_03_DP	34	DQS3
(33,67) CPU2_M_CH3_DQS_02_DN	24	DQS2_N
(33,67) CPU2_M_CH3_DQS_02_DP	25	DQS2
(33,67) CPU2_M_CH3_DQS_01_DN	15	DQS1_N
(33,67) CPU2_M_CH3_DQS_01_DP	16	DQS1
(33,67) CPU2_M_CH3_DQS_00_DN	6	DQS0_N
(33,67) CPU2_M_CH3_DQS_00_DP	7	DQS0
(33,67) CPU2_M_CH3_PERR_N	53	ERR_OUT_N/NC
(33,67) CPU2_M_CH3_MA_PAR	68	PAR_IN/NC
(33,67) CPU2_M_CH3_MA_PAR	167	NC/TEST

EVENT_N/NC
RESET_N

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DDR3-240-ATH40H26A-DELL

SPD = 0xA8
TSOD = 0x38

DO63	234	CPU2_M_CH3_DQ_63 (33,67)
DO62	233	CPU2_M_CH3_DQ_62 (33,67)
DO61	228	CPU2_M_CH3_DQ_61 (33,67)
DO60	227	CPU2_M_CH3_DQ_60 (33,67)
DO59	114	CPU2_M_CH3_DQ_59 (33,67)
DO58	109	CPU2_M_CH3_DQ_58 (33,67)
DO57	108	CPU2_M_CH3_DQ_57 (33,67)
DO56	225	CPU2_M_CH3_DQ_56 (33,67)
DO55	224	CPU2_M_CH3_DQ_55 (33,67)
DO54	224	CPU2_M_CH3_DQ_54 (33,67)
DO53	219	CPU2_M_CH3_DQ_53 (33,67)
DO52	218	CPU2_M_CH3_DQ_52 (33,67)
DO51	105	CPU2_M_CH3_DQ_51 (33,67)
DO50	100	CPU2_M_CH3_DQ_50 (33,67)
DO49	99	CPU2_M_CH3_DQ_49 (33,67)
DO48	216	CPU2_M_CH3_DQ_48 (33,67)
DO47	215	CPU2_M_CH3_DQ_47 (33,67)
DO46	210	CPU2_M_CH3_DQ_46 (33,67)
DO45	209	CPU2_M_CH3_DQ_45 (33,67)
DO44	97	CPU2_M_CH3_DQ_44 (33,67)
DO43	96	CPU2_M_CH3_DQ_43 (33,67)
DO42	91	CPU2_M_CH3_DQ_42 (33,67)
DO41	90	CPU2_M_CH3_DQ_41 (33,67)
DO40	207	CPU2_M_CH3_DQ_40 (33,67)
DO39	206	CPU2_M_CH3_DQ_39 (33,67)
DO38	201	CPU2_M_CH3_DQ_38 (33,67)
DO37	200	CPU2_M_CH3_DQ_37 (33,67)
DO36	88	CPU2_M_CH3_DQ_36 (33,67)
DO35	87	CPU2_M_CH3_DQ_35 (33,67)
DO34	82	CPU2_M_CH3_DQ_34 (33,67)
DO33	81	CPU2_M_CH3_DQ_33 (33,67)
DO32	156	CPU2_M_CH3_DQ_32 (33,67)
DO31	155	CPU2_M_CH3_DQ_31 (33,67)
DO30	149	CPU2_M_CH3_DQ_30 (33,67)
DO29	147	CPU2_M_CH3_DQ_29 (33,67)
DO28	146	CPU2_M_CH3_DQ_28 (33,67)
DO27	36	CPU2_M_CH3_DQ_27 (33,67)
DO26	31	CPU2_M_CH3_DQ_26 (33,67)
DO25	30	CPU2_M_CH3_DQ_25 (33,67)
DO24	147	CPU2_M_CH3_DQ_24 (33,67)
DO23	141	CPU2_M_CH3_DQ_23 (33,67)
DO22	141	CPU2_M_CH3_DQ_22 (33,67)
DO21	140	CPU2_M_CH3_DQ_21 (33,67)
DO20	28	CPU2_M_CH3_DQ_20 (33,67)
DO19	27	CPU2_M_CH3_DQ_19 (33,67)
DO18	22	CPU2_M_CH3_DQ_18 (33,67)
DO17	21	CPU2_M_CH3_DQ_17 (33,67)
DO16	138	CPU2_M_CH3_DQ_16 (33,67)
DO15	137	CPU2_M_CH3_DQ_15 (33,67)
DO14	132	CPU2_M_CH3_DQ_14 (33,67)
DO13	131	CPU2_M_CH3_DQ_13 (33,67)
DO12	131	CPU2_M_CH3_DQ_12 (33,67)
DO11	19	CPU2_M_CH3_DQ_11 (33,67)
DO10	18	CPU2_M_CH3_DQ_10 (33,67)
DO9	13	CPU2_M_CH3_DQ_09 (33,67)
DO8	12	CPU2_M_CH3_DQ_08 (33,67)
DO7	129	CPU2_M_CH3_DQ_07 (33,67)
DO6	128	CPU2_M_CH3_DQ_06 (33,67)
DO5	123	CPU2_M_CH3_DQ_05 (33,67)
DO4	122	CPU2_M_CH3_DQ_04 (33,67)
DO3	10	CPU2_M_CH3_DQ_03 (33,67)
DO2	9	CPU2_M_CH3_DQ_02 (33,67)
DO1	4	CPU2_M_CH3_DQ_01 (33,67)
DO0	3	CPU2_M_CH3_DQ_00 (33,67)
VTT_120	120	
VTT_240	240	
VTT_48/NC	48	
VTT_49/NC	49	
VDD_51	51	
VDD_54	54	
VDD_57	57	
VDD_60	60	
VDD_62	62	
VDD_65	65	
VDD_66	66	
VDD_69	69	
VDD_72	72	
VDD_75	75	
VDD_78	78	
VDD_170	170	
VDD_173	173	
VDD_176	176	
VDD_179	179	
VDD_182	182	
VDD_183	183	
VDD_186	186	
VDD_189	189	
VDD_191	191	
VDD_194	194	
VDD_197	197	



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V_MEM_VTT_CPU2

V_MEM_VDD_CPU2

FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)

Hon Hai Precision Ind. Co., Ltd.

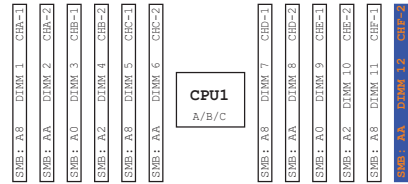
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Document Number: 01015C800-000-G
PCB P/N: 01015C800-000-G

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DIMM population



Harbor City is connected to DIMM Slot Directly.
R1123 49.9ohm
R0402H0_4
(63.64,66,69) I2C_CPU2_C23_SDA
(63.64,66,69) I2C_CPU2_C23_SCL
+3.3V SA=101
C581 0.1uF
+/-10%
C0402H0_55
X7R
16V

(60,66) CPU2_M_CH3_CA_VREF
(66,69) CPU2_M_CH3_DQ_VREF
(33) CPU2_M_CH3_ODT_3
(33) CPU2_M_CH3_ODT_2

(33,66) CPU2_M_CH3_ECC_7
(33,66) CPU2_M_CH3_ECC_6
(33,66) CPU2_M_CH3_ECC_5
(33,66) CPU2_M_CH3_ECC_4
(33,66) CPU2_M_CH3_ECC_3
(33,66) CPU2_M_CH3_ECC_2
(33,66) CPU2_M_CH3_ECC_1
(33,66) CPU2_M_CH3_ECC_0

(33,66) CPU2_M_CH3_DQS_17_DN
(33,66) CPU2_M_CH3_DQS_17_DP
(33,66) CPU2_M_CH3_DQS_16_DN
(33,66) CPU2_M_CH3_DQS_16_DP
(33,66) CPU2_M_CH3_DQS_15_DN
(33,66) CPU2_M_CH3_DQS_15_DP
(33,66) CPU2_M_CH3_DQS_14_DN
(33,66) CPU2_M_CH3_DQS_14_DP
(33,66) CPU2_M_CH3_DQS_13_DN
(33,66) CPU2_M_CH3_DQS_13_DP
(33,66) CPU2_M_CH3_DQS_12_DN
(33,66) CPU2_M_CH3_DQS_12_DP
(33,66) CPU2_M_CH3_DQS_11_DN
(33,66) CPU2_M_CH3_DQS_11_DP
(33,66) CPU2_M_CH3_DQS_10_DN
(33,66) CPU2_M_CH3_DQS_10_DP
(33,66) CPU2_M_CH3_DQS_09_DN
(33,66) CPU2_M_CH3_DQS_09_DP
(33,66) CPU2_M_CH3_DQS_08_DN
(33,66) CPU2_M_CH3_DQS_08_DP
(33,66) CPU2_M_CH3_DQS_07_DN
(33,66) CPU2_M_CH3_DQS_07_DP
(33,66) CPU2_M_CH3_DQS_06_DN
(33,66) CPU2_M_CH3_DQS_06_DP
(33,66) CPU2_M_CH3_DQS_05_DN
(33,66) CPU2_M_CH3_DQS_05_DP
(33,66) CPU2_M_CH3_DQS_04_DN
(33,66) CPU2_M_CH3_DQS_04_DP
(33,66) CPU2_M_CH3_DQS_03_DN
(33,66) CPU2_M_CH3_DQS_03_DP
(33,66) CPU2_M_CH3_DQS_02_DN
(33,66) CPU2_M_CH3_DQS_02_DP
(33,66) CPU2_M_CH3_DQS_01_DN
(33,66) CPU2_M_CH3_DQS_01_DP
(33,66) CPU2_M_CH3_DQS_00_DN
(33,66) CPU2_M_CH3_DQS_00_DP

(33,66) CPU2_M_CH3_PERR_N
(33,66) CPU2_M_CH3_MA_PAR

NC_CPU2_CH3_D1_P167

ERR_OUT_N/NC
PAR_IN/NC
NC/TEST

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DIMM12A

BA2
BA1
BA0
A15/NC
A14
A13
A12_BC_N
A11
A10/AP
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0

(33) CPU2_M_CH3_CS_7_N
(33) CPU2_M_CH3_CS_6_N
(33) CPU2_M_CH3_CS_5_N
(33) CPU2_M_CH3_CS_4_N
(33,66) CPU2_M_CH3_RAS_N
(33,66) CPU2_M_CH3_CAS_N
(33,66) CPU2_M_CH3_WE_N
(33) CPU2_M_CH3_CK_3_DP
(33) CPU2_M_CH3_CK_3_DN
(33) CPU2_M_CH3_CK_1_DP
(33) CPU2_M_CH3_CK_1_DN
(33) CPU2_M_CH3_CKE_3
(33) CPU2_M_CH3_CKE_2

S3_N/NC
S2_N/NC
S1_N/NC
S0_N
RAS_N
CAS_N
WE_N
CK_3_N
CK_1_N
CK_0_N
CKE1/NC
CKE0

SDA
SCL
SA2
SA1
SA0
VDDSPD
VREFCA
VREFDQ
ODT1/NC
ODT0

CB7/NC
CB6/NC
CB5/NC
CB4/NC
CB3/NC
CB2/NC
CB1/NC
CB0/NC

NC/DQS17_N/TDQS17_N
DM8/DQS17/TDQS17/NC
NC/DQS16_N/TDQS16_N
DM7/DQS16/TDQS16/NC
NC/DQS15_N/TDQS15_N
DM6/DQS15/TDQS15/NC
NC/DQS14_N/TDQS14_N
DM5/DQS14/TDQS14/NC
NC/DQS13_N/TDQS13_N
DM4/DQS13/TDQS13/NC
NC/DQS12_N/TDQS12_N
DM3/DQS12/TDQS12/NC
NC/DQS11_N/TDQS11_N
DM2/DQS11/TDQS11/NC
NC/DQS10_N/TDQS10_N
DM1/DQS10/TDQS10/NC
NC/DQS9_N/TDQS9_N
DM0/DQS9/TDQS9/NC
DQS8_N
DQS7_N
DQS6_N
DQS5_N
DQS4_N
DQS3_N
DQS2_N
DQS1_N
DQS0_N
DQS0

VTT_120
VTT_240
VTT_48/NC
VTT_49/NC
VDD_51
VDD_54
VDD_57
VDD_60
VDD_62
VDD_65
VDD_66
VDD_69
VDD_72
VDD_75
VDD_78
VDD_170
VDD_173
VDD_176
VDD_179
VDD_182
VDD_183
VDD_186
VDD_189
VDD_191
VDD_194
VDD_197

EVENT_N/NC
RESET_N

DIMM_TEMP_EVENT_N (47,48,50,51,53,54,60,61,63,64,66,153)
CPU2_M_CH23_RST_N (29,63,64,66)

DIMM12B

VSS_124
VSS_127
VSS_130
VSS_133
VSS_136
VSS_139
VSS_142
VSS_145
VSS_148
VSS_151
VSS_154
VSS_157
VSS_160
VSS_163
VSS_166
VSS_169
VSS_172
VSS_175
VSS_178
VSS_181
VSS_184
VSS_187
VSS_190
VSS_193
VSS_196
VSS_199
VSS_202
VSS_205
VSS_208
VSS_211
VSS_214
VSS_217
VSS_220
VSS_223
VSS_226
VSS_229
VSS_232
VSS_235
VSS_239

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V_MEM_VTT_CPU2

V_MEM_VDD_CPU2

Harbor City use 0805 47uF x5.

C1778 10uF
+/-20%
C0603H0_9
X5R
6.3V

C1779 10uF
+/-20%
C0603H0_9
X5R
6.3V

C1781 10uF
+/-20%
C0603H0_9
X5R
6.3V

C1780 10uF
+/-20%
C0603H0_9
X5R
6.3V

C519 10uF
+/-20%
C0603H0_9
X5R
6.3V

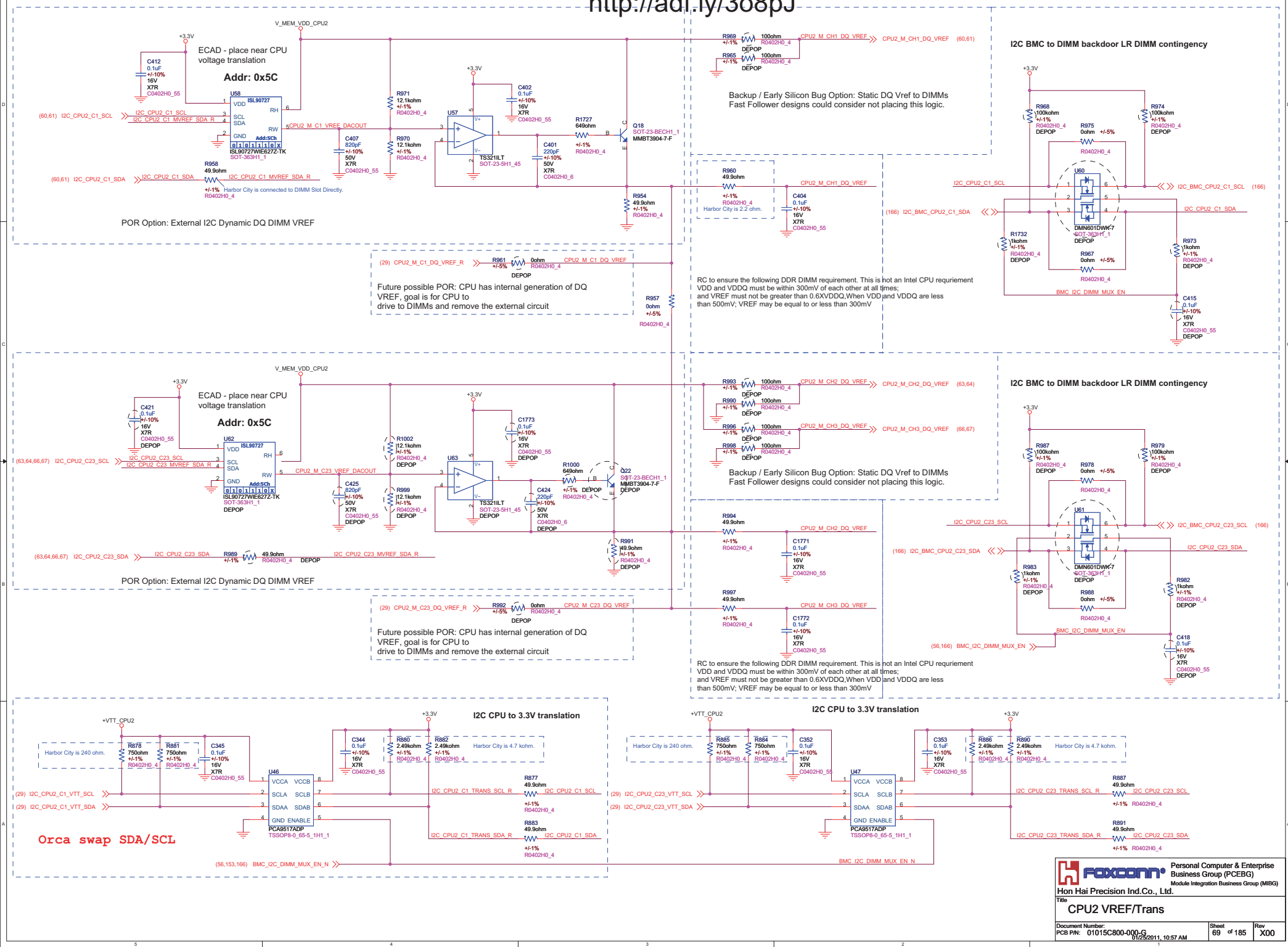
C509 10uF
+/-20%
C0603H0_9
X5R
6.3V

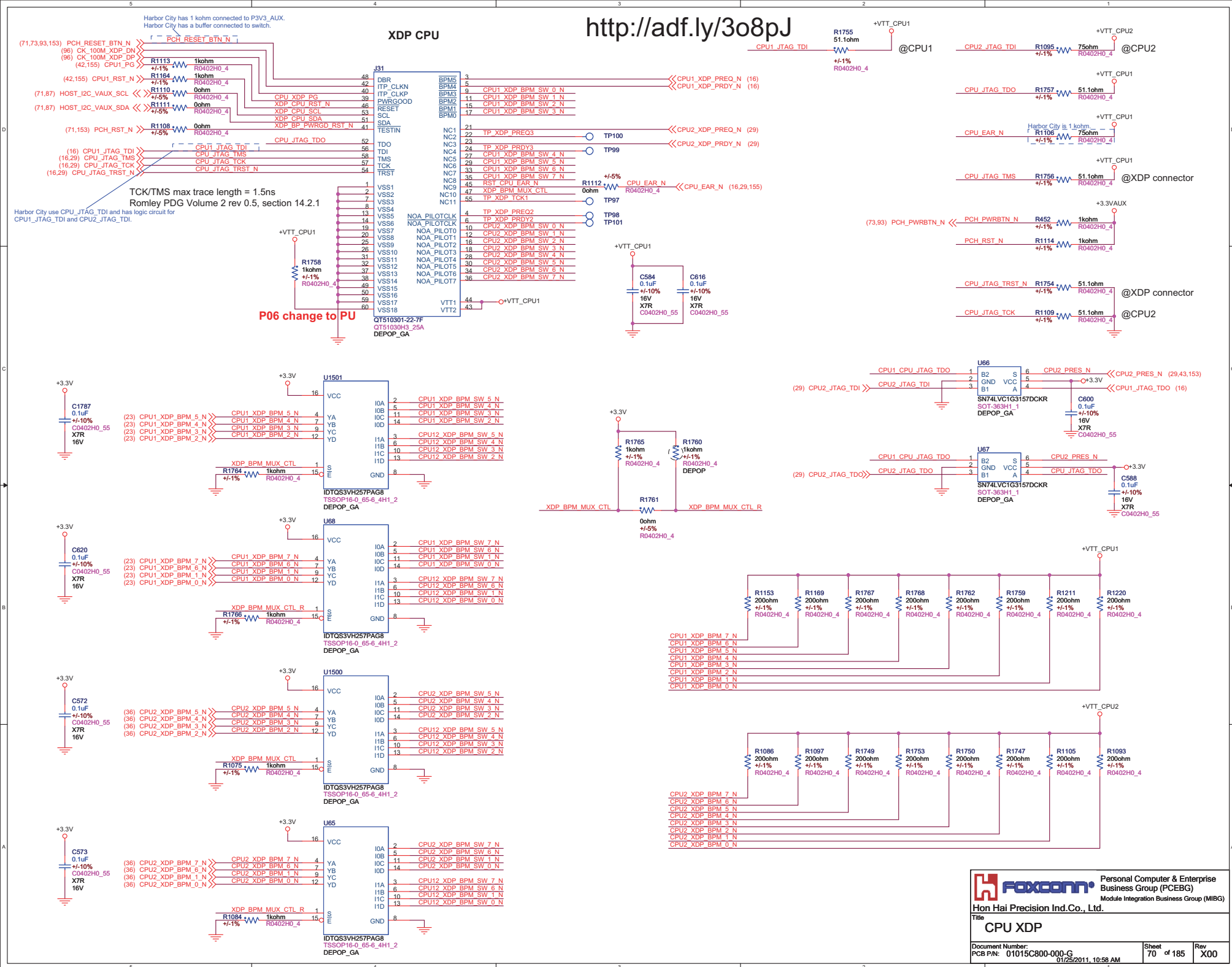
C499 10uF
+/-20%
C0603H0_9
X5R
6.3V

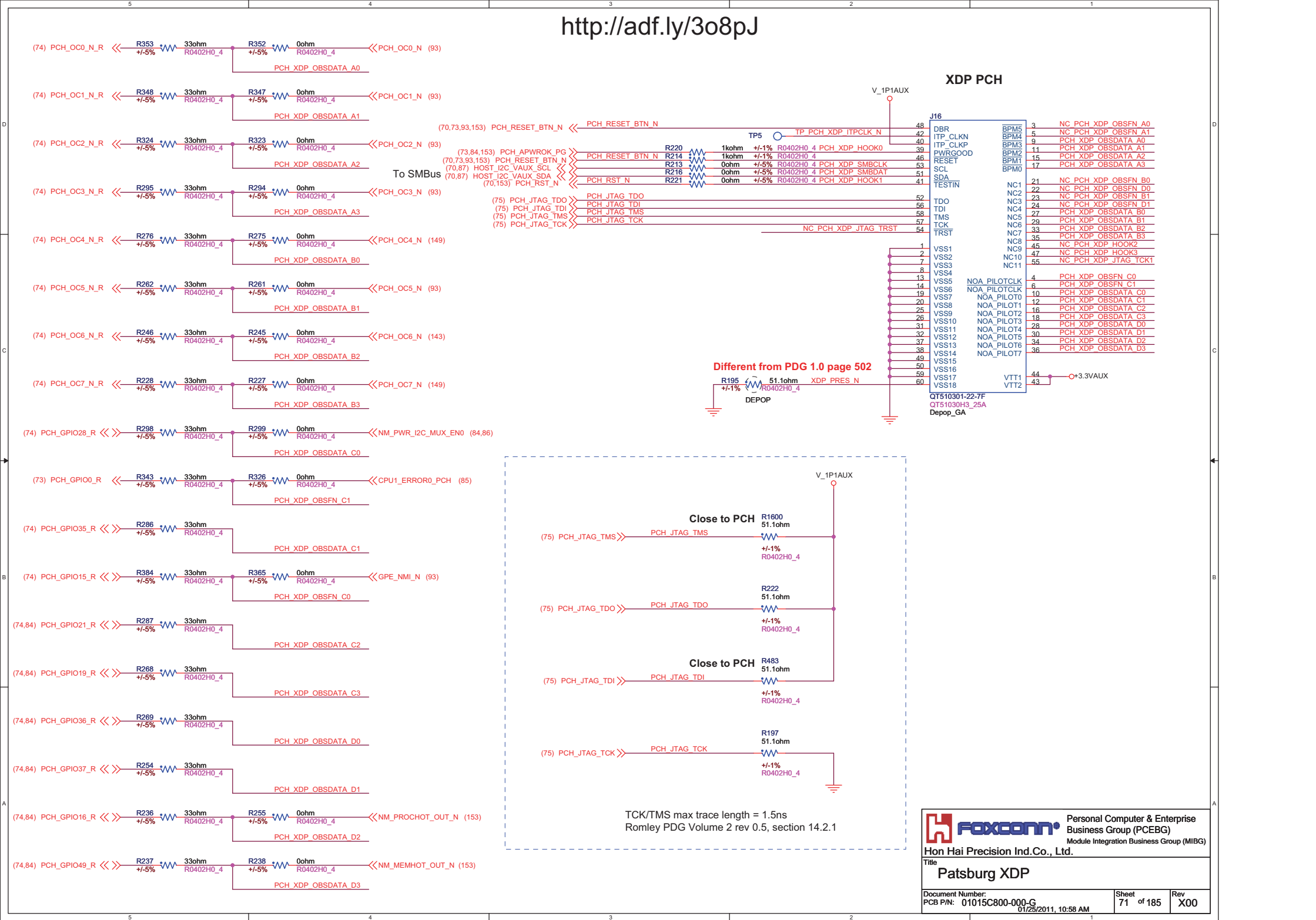
C514 10uF
+/-20%
C0603H0_9
X5R
6.3V

SPD = 0xAA
TSOD = 0x3A

FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)
Hon Hai Precision Ind. Co., Ltd.
Title
CPU2 CH3 DIMM1
Document Number:
PCB P/N: 01015C800-000-G
01/25/2011, 10:57 AM
Sheet 67 of 185
Rev X00





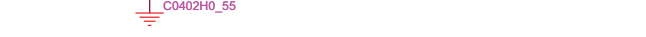
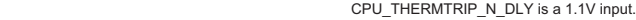


CPU1 ECAD: Place near PCIe connector

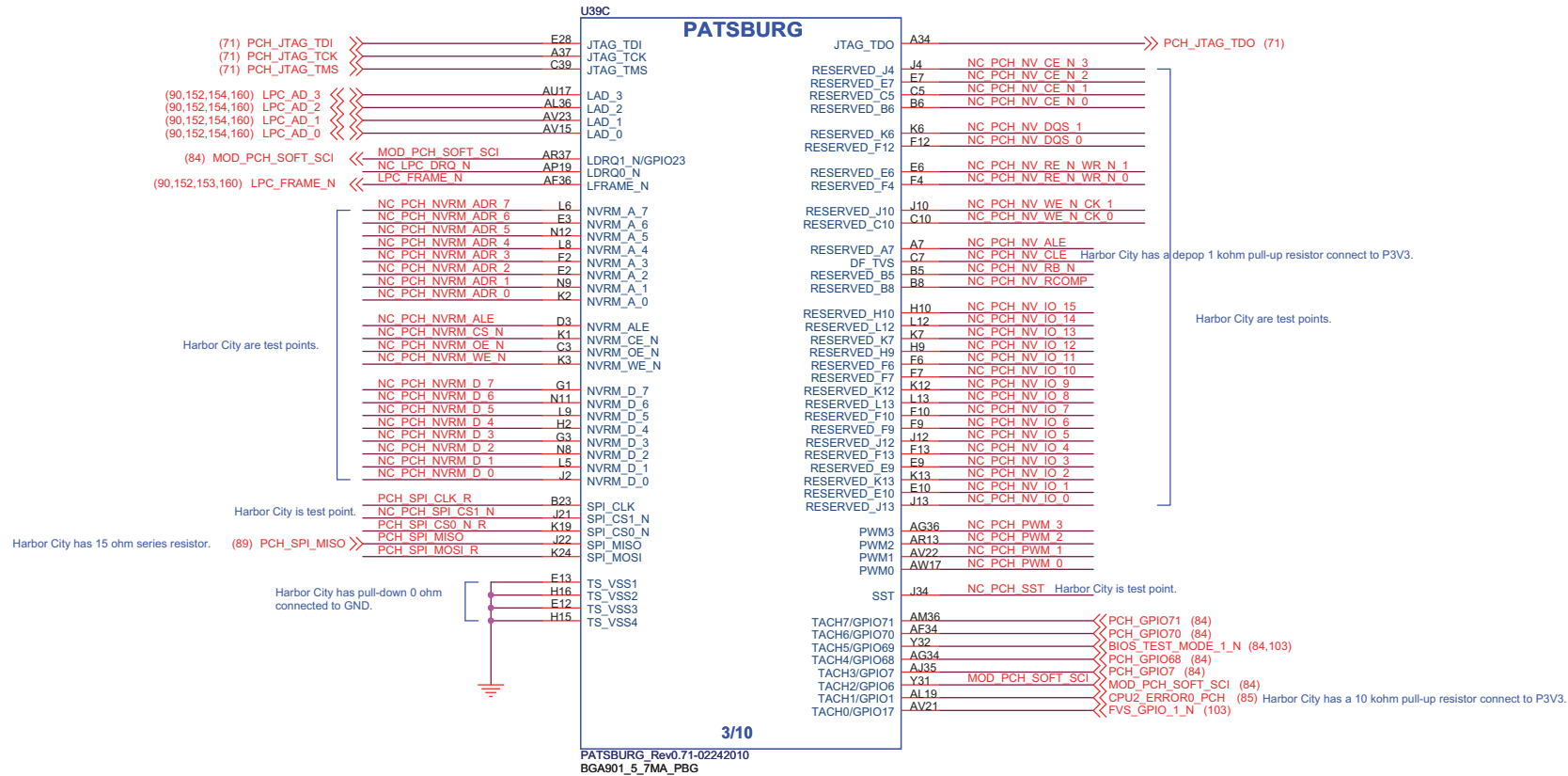
(22) PE_CPU1_3D_SB_15_C_DP	C160	220nF +/-10% 16V X7R	PE_CPU1_3D_SB_15_DP (143)
(22) PE_CPU1_3D_SB_14_C_DP	C167	220nF +/-10% 16V X7R	PE_CPU1_3D_SB_14_DP (143)
(22) PE_CPU1_3D_SB_13_C_DP	C178	220nF +/-10% 16V X7R	PE_CPU1_3D_SB_13_DP (143)
(22) PE_CPU1_3D_SB_12_C_DP	C196	220nF +/-10% 16V X7R	PE_CPU1_3D_SB_12_DP (143)
(22) PE_CPU1_3D_SB_15_C_DN	C162	220nF +/-10% 16V X7R	PE_CPU1_3D_SB_15_DN (143)
(22) PE_CPU1_3D_SB_14_C_DN	C169	220nF +/-10% 16V X7R	PE_CPU1_3D_SB_14_DN (143)
(22) PE_CPU1_3D_SB_13_C_DN	C182	220nF +/-10% 16V X7R	PE_CPU1_3D_SB_13_DN (143)
(22) PE_CPU1_3D_SB_12_C_DN	C200	220nF +/-10% 16V X7R	PE_CPU1_3D_SB_12_DN (143)
(22) PE_CPU1_3C_SB_11_C_DP	C207	220nF +/-10% 16V X7R	PE_CPU1_3C_SB_11_DP (143)
(22) PE_CPU1_3C_SB_10_C_DP	C219	220nF +/-10% 16V X7R	PE_CPU1_3C_SB_10_DP (143)
(22) PE_CPU1_3C_SB_9_C_DP	C231	220nF +/-10% 16V X7R	PE_CPU1_3C_SB_9_DP (143)
(22) PE_CPU1_3C_SB_8_C_DP	C238	220nF +/-10% 16V X7R	PE_CPU1_3C_SB_8_DP (143)
(22) PE_CPU1_3C_SB_11_C_DN	C213	220nF +/-10% 16V X7R	PE_CPU1_3C_SB_11_DN (143)
(22) PE_CPU1_3C_SB_10_C_DN	C222	220nF +/-10% 16V X7R	PE_CPU1_3C_SB_10_DN (143)
(22) PE_CPU1_3C_SB_9_C_DN	C233	220nF +/-10% 16V X7R	PE_CPU1_3C_SB_9_DN (143)
(22) PE_CPU1_3C_SB_8_C_DN	C244	220nF +/-10% 16V X7R	PE_CPU1_3C_SB_8_DN (143)
(22) PE_CPU1_3B_SB_7_C_DP	C250	220nF +/-10% 16V X7R	PE_CPU1_3B_SB_7_DP (143)
(22) PE_CPU1_3B_SB_6_C_DP	C267	220nF +/-10% 16V X7R	PE_CPU1_3B_SB_6_DP (143)
(22) PE_CPU1_3B_SB_5_C_DP	C274	220nF +/-10% 16V X7R	PE_CPU1_3B_SB_5_DP (143)
(22) PE_CPU1_3B_SB_4_C_DP	C281	220nF +/-10% 16V X7R	PE_CPU1_3B_SB_4_DP (143)
(22) PE_CPU1_3B_SB_7_C_DN	C256	220nF +/-10% 16V X7R	PE_CPU1_3B_SB_7_DN (143)
(22) PE_CPU1_3B_SB_6_C_DN	C272	220nF +/-10% 16V X7R	PE_CPU1_3B_SB_6_DN (143)
(22) PE_CPU1_3B_SB_5_C_DN	C277	220nF +/-10% 16V X7R	PE_CPU1_3B_SB_5_DN (143)
(22) PE_CPU1_3B_SB_4_C_DN	C285	220nF +/-10% 16V X7R	PE_CPU1_3B_SB_4_DN (143)
(22) PE_CPU1_3A_SB_3_C_DP	C290	220nF +/-10% 16V X7R	PE_CPU1_3A_SB_3_DP (143)
(22) PE_CPU1_3A_SB_2_C_DP	C323	220nF +/-10% 16V X7R	PE_CPU1_3A_SB_2_DP (143)
(22) PE_CPU1_3A_SB_1_C_DP	C328	220nF +/-10% 16V X7R	PE_CPU1_3A_SB_1_DP (143)
(22) PE_CPU1_3A_SB_0_C_DP	C341	220nF +/-10% 16V X7R	PE_CPU1_3A_SB_0_DP (143)
(22) PE_CPU1_3A_SB_3_C_DN	C308	220nF +/-10% 16V X7R	PE_CPU1_3A_SB_3_DN (143)
(22) PE_CPU1_3A_SB_2_C_DN	C325	220nF +/-10% 16V X7R	PE_CPU1_3A_SB_2_DN (143)
(22) PE_CPU1_3A_SB_1_C_DN	C333	220nF +/-10% 16V X7R	PE_CPU1_3A_SB_1_DN (143)
(22) PE_CPU1_3A_SB_0_C_DN	C343	220nF +/-10% 16V X7R	PE_CPU1_3A_SB_0_DN (143)

CPU2 ECAD: Place near PCIe connector

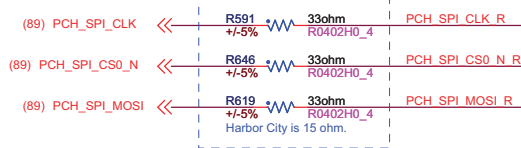
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(35) PE_CPU2_3D_SB_14_C_DP	C426	220nF +/-10% 16V X7R	PE_CPU2_3D_SB_14_DP (142)
(35) PE_CPU2_3D_SB_13_C_DP	C422	220nF +/-10% 16V X7R	PE_CPU2_3D_SB_13_DP (142)
(35) PE_CPU2_3D_SB_12_C_DP	C417	220nF +/-10% 16V X7R	PE_CPU2_3D_SB_12_DP (142)
(35) PE_CPU2_3D_SB_15_C_DN	C431	220nF +/-10% 16V X7R	PE_CPU2_3D_SB_15_DN (142)
(35) PE_CPU2_3D_SB_14_C_DN	C428	220nF +/-10% 16V X7R	PE_CPU2_3D_SB_14_DN (142)
(35) PE_CPU2_3D_SB_13_C_DN	C423	220nF +/-10% 16V X7R	PE_CPU2_3D_SB_13_DN (142)
(35) PE_CPU2_3D_SB_12_C_DN	C420	220nF +/-10% 16V X7R	PE_CPU2_3D_SB_12_DN (142)
(35) PE_CPU2_3C_SB_11_C_DP	C414	220nF +/-10% 16V X7R	PE_CPU2_3C_SB_11_DP (142)
(35) PE_CPU2_3C_SB_10_C_DP	C409	220nF +/-10% 16V X7R	PE_CPU2_3C_SB_10_DP (142)
(35) PE_CPU2_3C_SB_9_C_DP	C400	220nF +/-10% 16V X7R	PE_CPU2_3C_SB_9_DP (142)
(35) PE_CPU2_3C_SB_8_C_DP	C397	220nF +/-10% 16V X7R	PE_CPU2_3C_SB_8_DP (142)
(35) PE_CPU2_3C_SB_11_C_DN	C416	220nF +/-10% 16V X7R	PE_CPU2_3C_SB_11_DN (142)
(35) PE_CPU2_3C_SB_10_C_DN	C410	220nF +/-10% 16V X7R	PE_CPU2_3C_SB_10_DN (142)
(35) PE_CPU2_3C_SB_9_C_DN	C403	220nF +/-10% 16V X7R	PE_CPU2_3C_SB_9_DN (142)
(35) PE_CPU2_3C_SB_8_C_DN	C398	220nF +/-10% 16V X7R	PE_CPU2_3C_SB_8_DN (142)
(35) PE_CPU2_3B_SB_7_C_DP	C390	220nF +/-10% 16V X7R	PE_CPU2_3B_SB_7_DP (142)
(35) PE_CPU2_3B_SB_6_C_DP	C384	220nF +/-10% 16V X7R	PE_CPU2_3B_SB_6_DP (142)
(35) PE_CPU2_3B_SB_5_C_DP	C372	220nF +/-10% 16V X7R	PE_CPU2_3B_SB_5_DP (142)
(35) PE_CPU2_3B_SB_4_C_DP	C365	220nF +/-10% 16V X7R	PE_CPU2_3B_SB_4_DP (142)
(35) PE_CPU2_3B_SB_7_C_DN	C394	220nF +/-10% 16V X7R	PE_CPU2_3B_SB_7_DN (142)
(35) PE_CPU2_3B_SB_6_C_DN	C387	220nF +/-10% 16V X7R	PE_CPU2_3B_SB_6_DN (142)
(35) PE_CPU2_3B_SB_5_C_DN	C378	220nF +/-10% 16V X7R	PE_CPU2_3B_SB_5_DN (142)
(35) PE_CPU2_3B_SB_4_C_DN	C366	220nF +/-10% 16V X7R	PE_CPU2_3B_SB_4_DN (142)
(35) PE_CPU2_3A_SB_3_C_DP	C351	220nF +/-10% 16V X7R	PE_CPU2_3A_SB_3_DP (142)
(35) PE_CPU2_3A_SB_2_C_DP	C348	220nF +/-10% 16V X7R	PE_CPU2_3A_SB_2_DP (142)
(35) PE_CPU2_3A_SB_1_C_DP	C339	220nF +/-10% 16V X7R	PE_CPU2_3A_SB_1_DP (142)
(35) PE_CPU2_3A_SB_0_C_DP	C327	220nF +/-10% 16V X7R	PE_CPU2_3A_SB_0_DP (142)
(35) PE_CPU2_3A_SB_3_C_DN	C357	220nF +/-10% 16V X7R	PE_CPU2_3A_SB_3_DN (142)
(35) PE_CPU2_3A_SB_2_C_DN	C347	220nF +/-10% 16V X7R	PE_CPU2_3A_SB_2_DN (142)
(35) PE_CPU2_3A_SB_1_C_DN	C342	220nF +/-10% 16V X7R	PE_CPU2_3A_SB_1_DN (142)
(35) PE_CPU2_3A_SB_0_C_DN	C331	220nF +/-10% 16V X7R	PE_CPU2_3A_SB_0_DN (142)
(34) PE_CPU2_1B_SB_7_C_DP	C44	220nF +/-10% 16V X7R	PE_CPU2_1B_SB_7_DP (143)
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(34) PE_CPU2_1B_SB_5_C_DP	C82	220nF +/-10% 16V X7R	PE_CPU2_1B_SB_5_DP (143)
(34) PE_CPU2_1B_SB_4_C_DP	C94	220nF +/-10% 16V X7R	PE_CPU2_1B_SB_4_DP (143)
(34) PE_CPU2_1B_SB_7_C_DN	C55	220nF +/-10% 16V X7R	PE_CPU2_1B_SB_7_DN (143)
(34) PE_CPU2_1B_SB_6_C_DN	C79	220nF +/-10% 16V X7R	PE_CPU2_1B_SB_6_DN (143)
(34) PE_CPU2_1B_SB_5_C_DN	C86	220nF +/-10% 16V X7R	PE_CPU2_1B_SB_5_DN (143)
(34) PE_CPU2_1B_SB_4_C_DN	C100	220nF +/-10% 16V X7R	PE_CPU2_1B_SB_4_DN (143)
(34) PE_CPU2_1A_SB_3_C_DP	C127	220nF +/-10% 16V X7R	PE_CPU2_1A_SB_3_DP (143)
(34) PE_CPU2_1A_SB_2_C_DP	C136	220nF +/-10% 16V X7R	PE_CPU2_1A_SB_2_DP (143)
(34) PE_CPU2_1A_SB_1_C_DP	C145	220nF +/-10% 16V X7R	PE_CPU2_1A_SB_1_DP (143)
(34) PE_CPU2_1A_SB_0_C_DP	C150	220nF +/-10% 16V X7R	PE_CPU2_1A_SB_0_DP (143)
(34) PE_CPU2_1A_SB_3_C_DN	C132	220nF +/-10% 16V X7R	PE_CPU2_1A_SB_3_DN (143)
(34) PE_CPU2_1A_SB_2_C_DN	C137	220nF +/-10% 16V X7R	PE_CPU2_1A_SB_2_DN (143)
(34) PE_CPU2_1A_SB_1_C_DN	C146	220nF +/-10% 16V X7R	PE_CPU2_1A_SB_1_DN (143)
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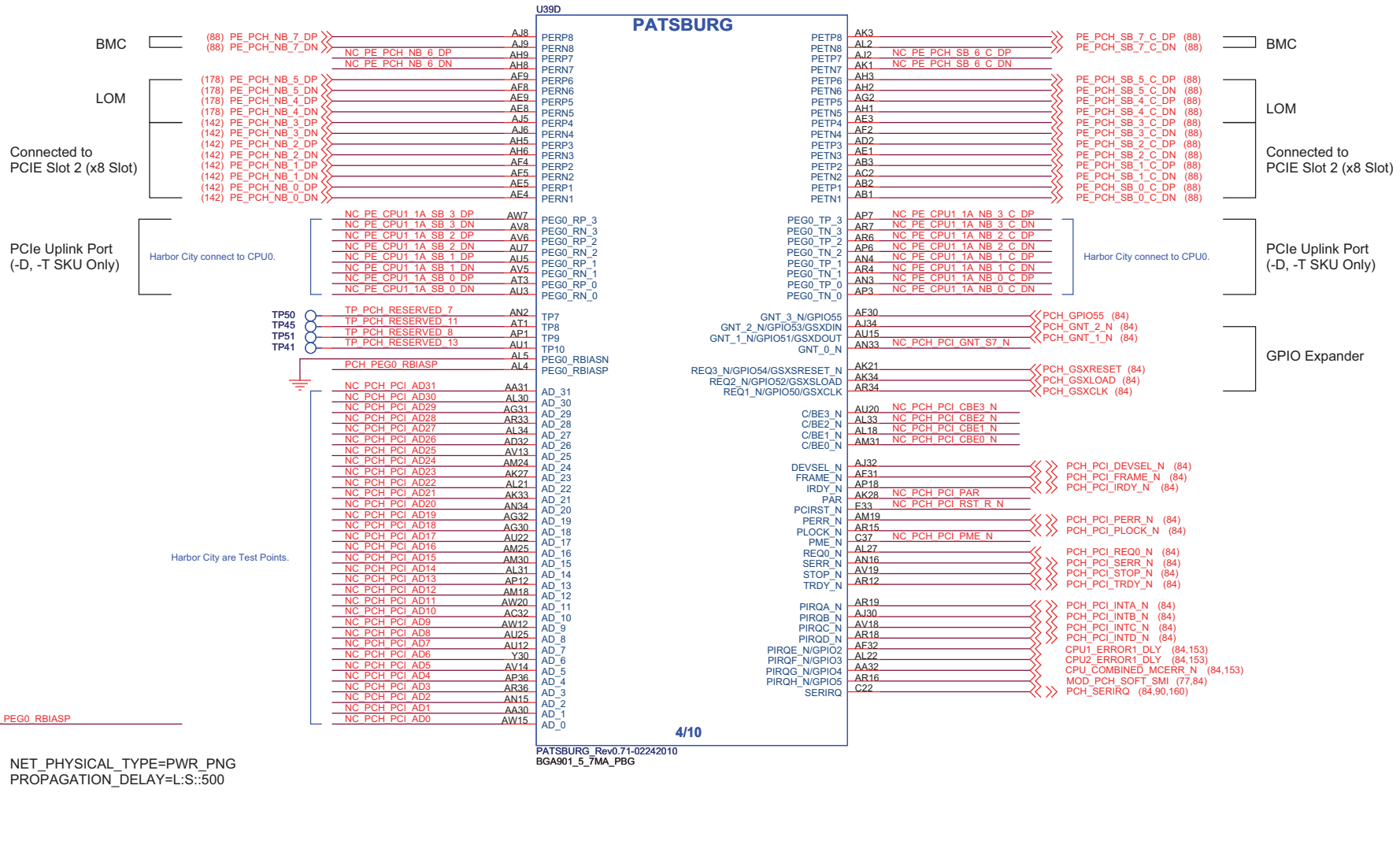


FOX ELECTRONICS 414LF-0.032768-1



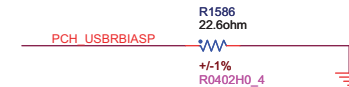
Intel recommend 15ohm for series resistor



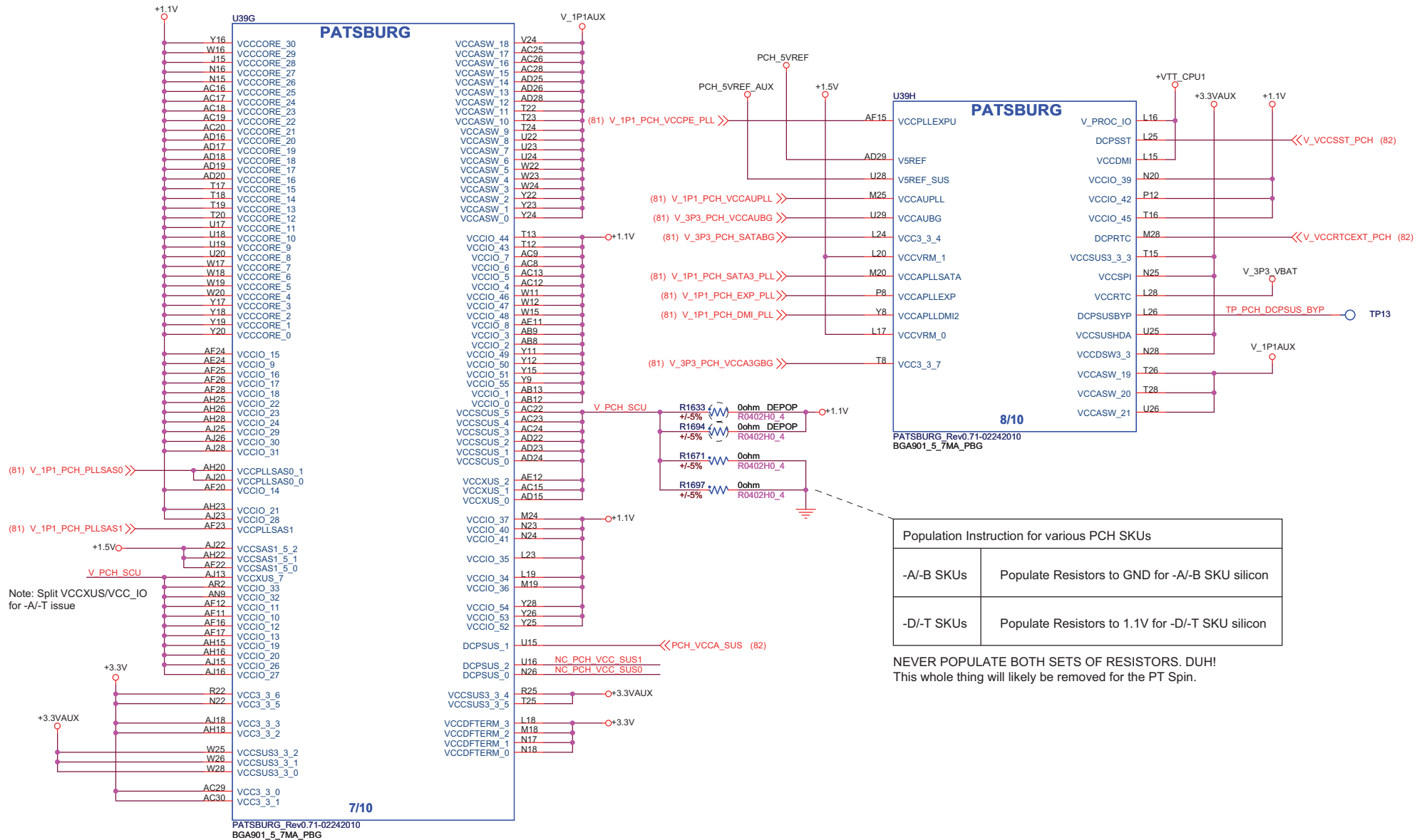


<http://adf.ly/3o8pJ>



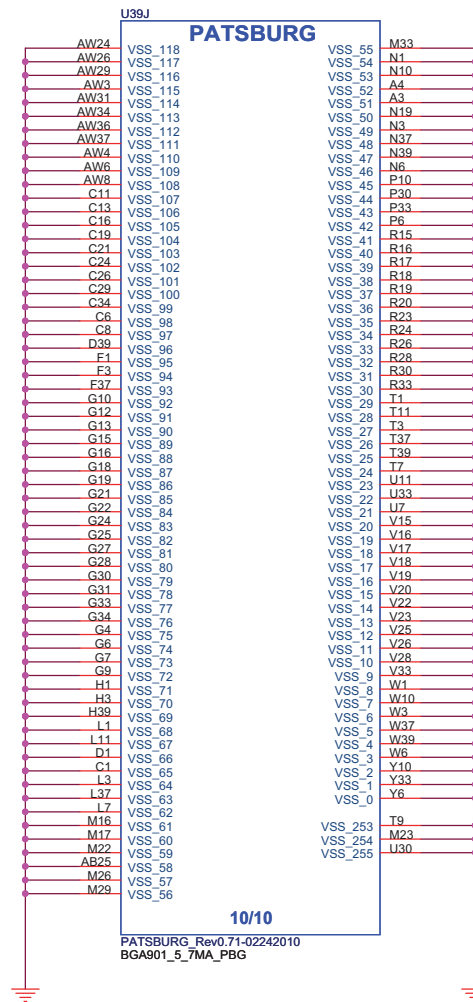
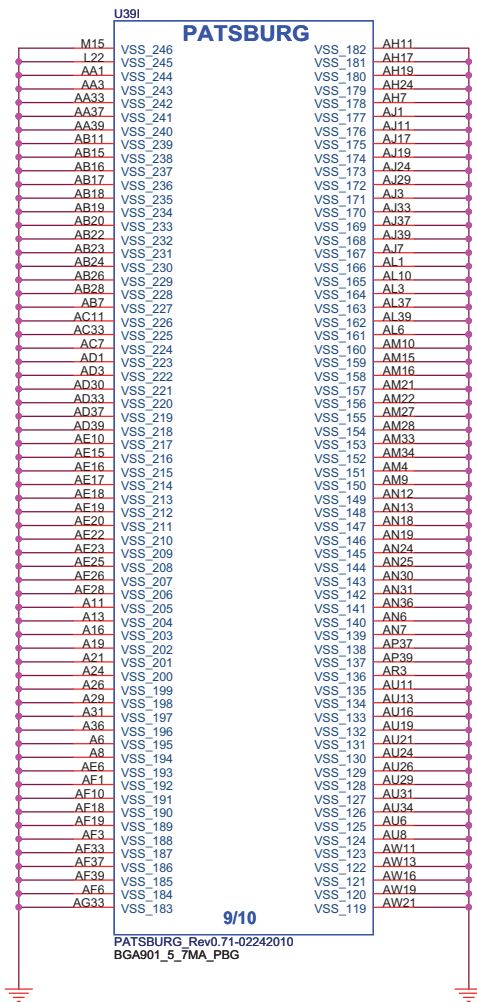


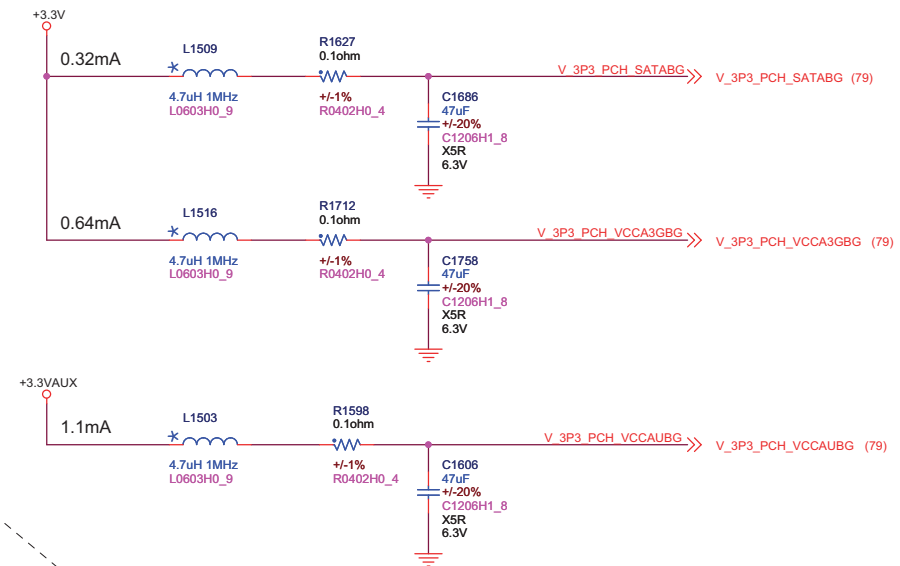
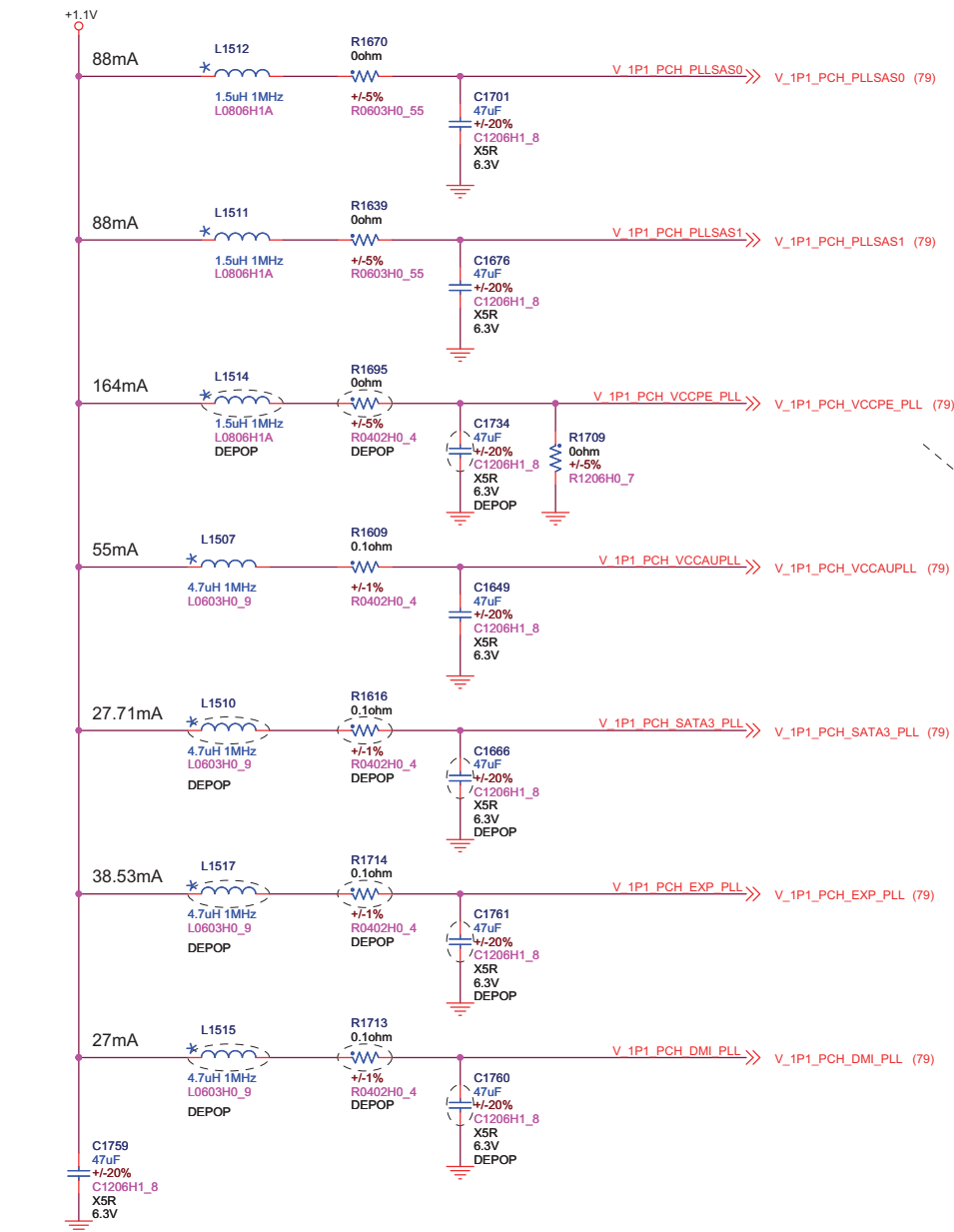
USB Port		Power	SDS	Over Current	Orca	Note
EHCI #1 OC[3:0]#	0	NA	NC		NC	Debug capability
	1	PCH_USB_PWR_1	REAR IO	OC0#	REAR IO	
	2	NA	BMC		NC	
	3	NA	NC		NC	
	4	NA	NC		NC	
	5	+5V	IDSDM		NC	
	6	NA	NC		NC	
EHCI #2 OC[7:4]#	7	PCH_USB_PWR_2	REAR IO	OC1#	NC	Debug capability
	8	NA	NC		Internal	
	9	NA	Front	OC4#	Front	
	10	NA	LEFT RISER	OC6#	IDSDM	
	11	NA	NC		REAR IO	
	12	NA	Front	OC7#	Front	
	13	NA	BMC		BMC	



Population Instruction for various PCH SKUs	
-A/-B SKUs	Populate Resistors to GND for -A/-B SKU silicon
-D/-T SKUs	Populate Resistors to 1.1V for -D/-T SKU silicon

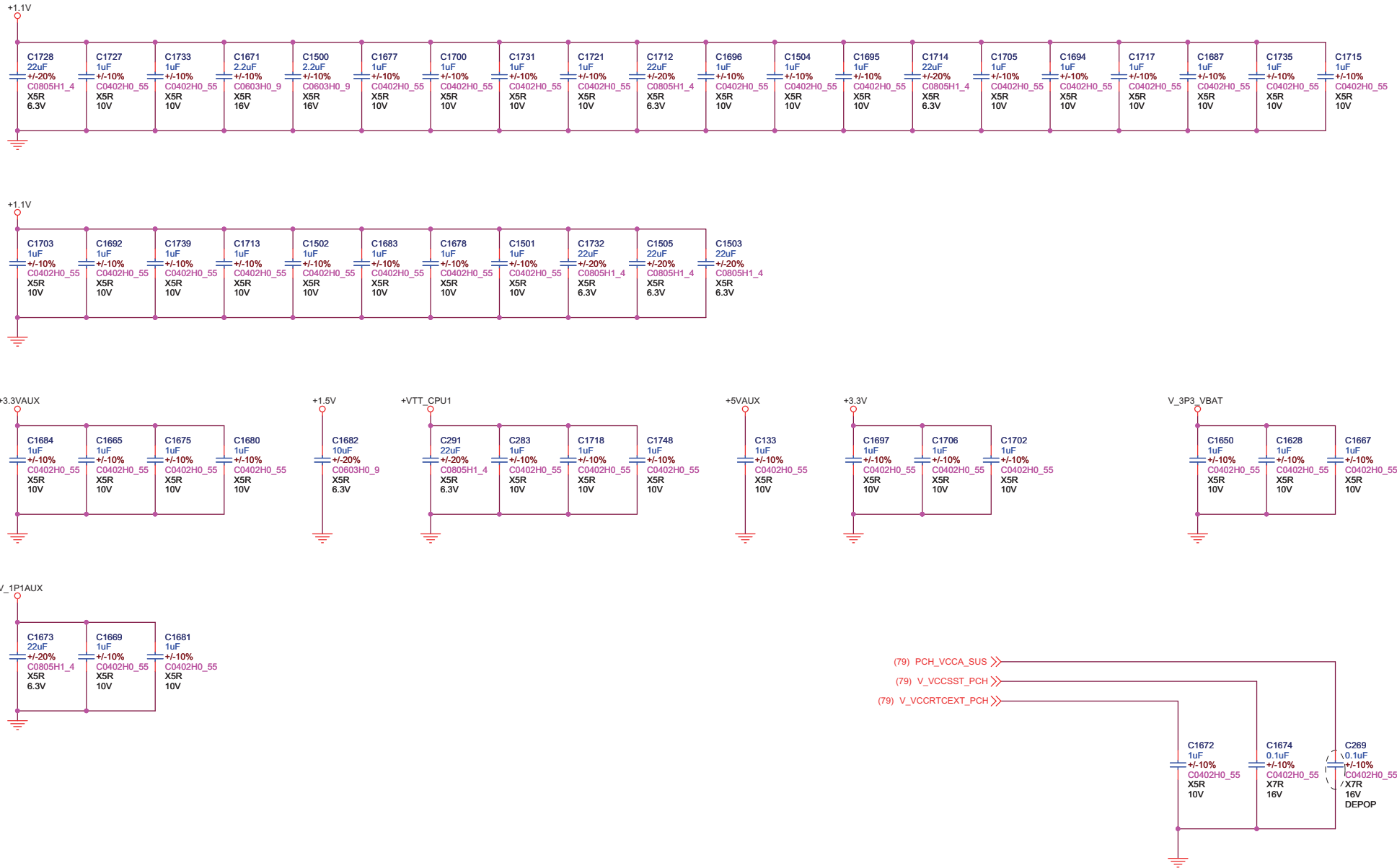
NEVER POPULATE BOTH SETS OF RESISTORS. DUH!
This whole thing will likely be removed for the PT Spin.

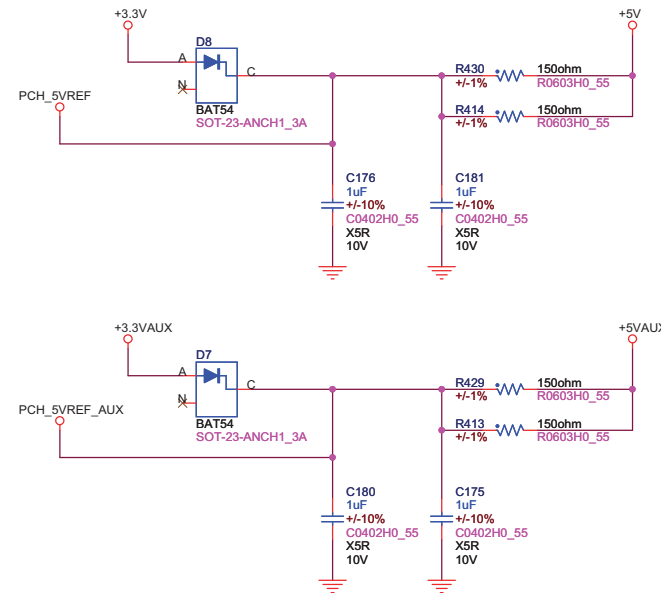




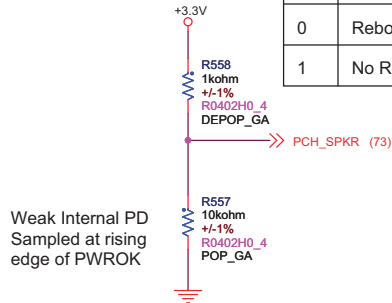
Population Instruction for various PCH SKUs	
-A/-B SKUs	Populate C2290 with a 0 ohm, depop R2452, L2021
-D/-T SKUs	Populate as shown in the schematic

Obviously do not create a 1.1V to ground short. Duh.
This whole thing will likely be removed for the PT Spin.



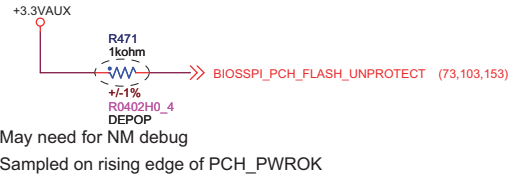


Val	Function
0	Reboot Mode
1	No Reboot Mode

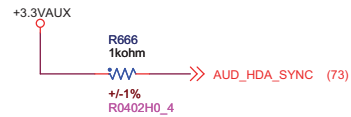


Flash Descriptor Override Strapping

Flash Descriptor security override DISABLED
Sampled on rising edge of PCH_PWROK



PLL VR Voltage Strapping



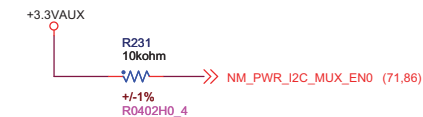
Set on-die VR to 1.5V
Sampled on rising edge of RSMRST#

DMI AC Coupling Strap



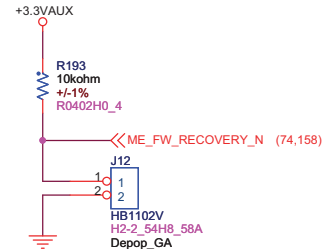
Low=AC Coupled, High/Open=DC Coupled
Sampled on rising edge of PCH_PWROK

PLL Voltage Regulator Enable



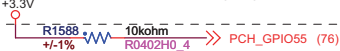
Set on-die PLL Voltage Regulator Enable
Sampled on rising edge of RSMRST#
Probably can be no-popped after NM backout stuff is settled down

Designers Note:
If you actually use this interface
make sure to change resistors
to 2K for max speed.



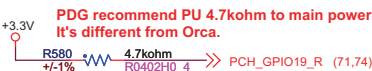
GPIO36 pull high 150k~200k ohm per MOW ww50.

Top-Block Swap Override High=Normal
Sampled on rising edge of PCH_PWROK



Boot Source Select [Always SPI]

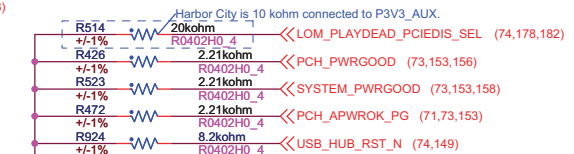
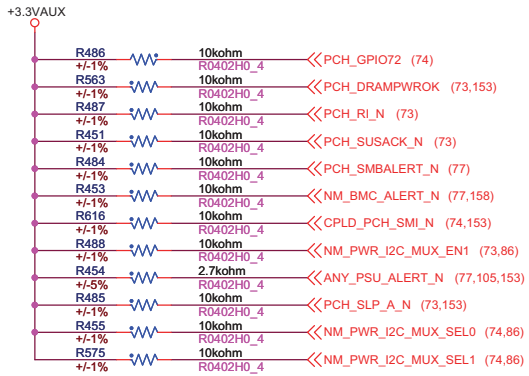
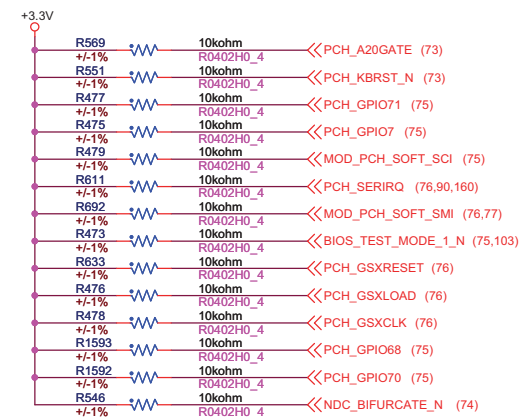
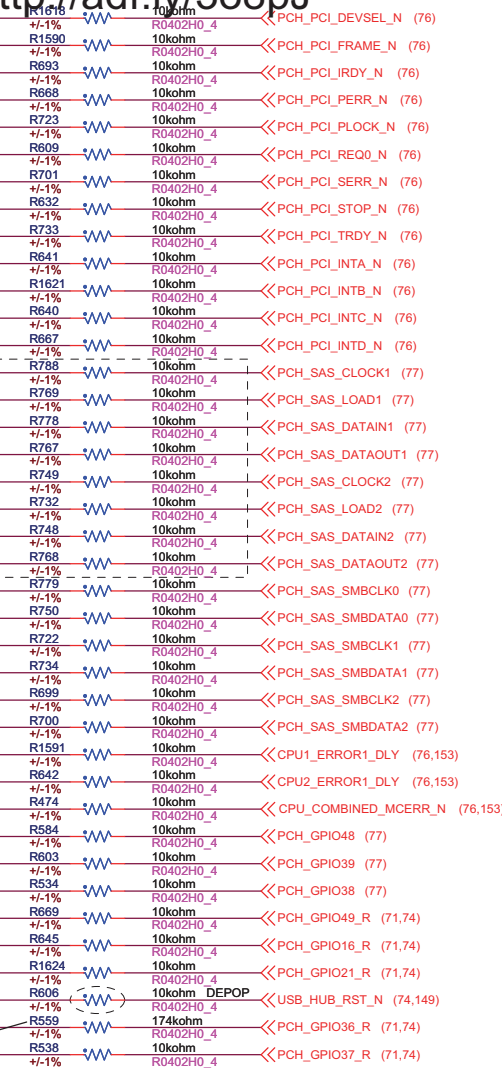
Sampled on rising edge of PCH_PWROK



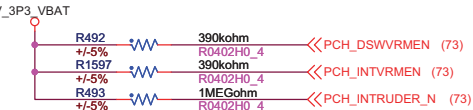
GPIO51/GNT1_N pull-high voltage is different from Orca (+3.3VAUX)



<http://adf.ly/3o8pJ>



Intel recommend PD 8.2k~10k ohm for PCH_PWRGOOD
Intel recommend PD 8.2k~10k ohm for SYSTEM_PWRGOOD
Intel recommend PD 8.2k~10k ohm for PCH_APWROK_PG



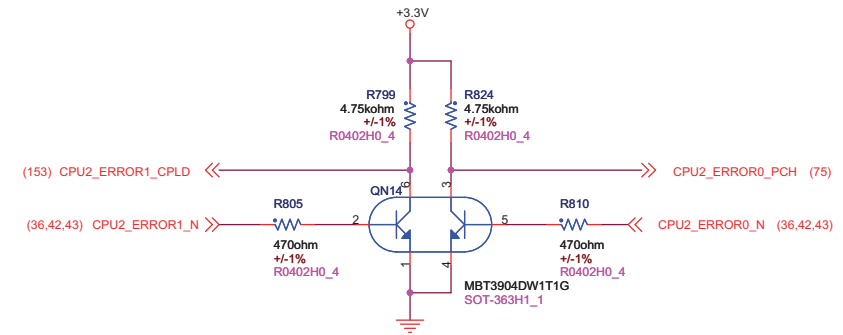
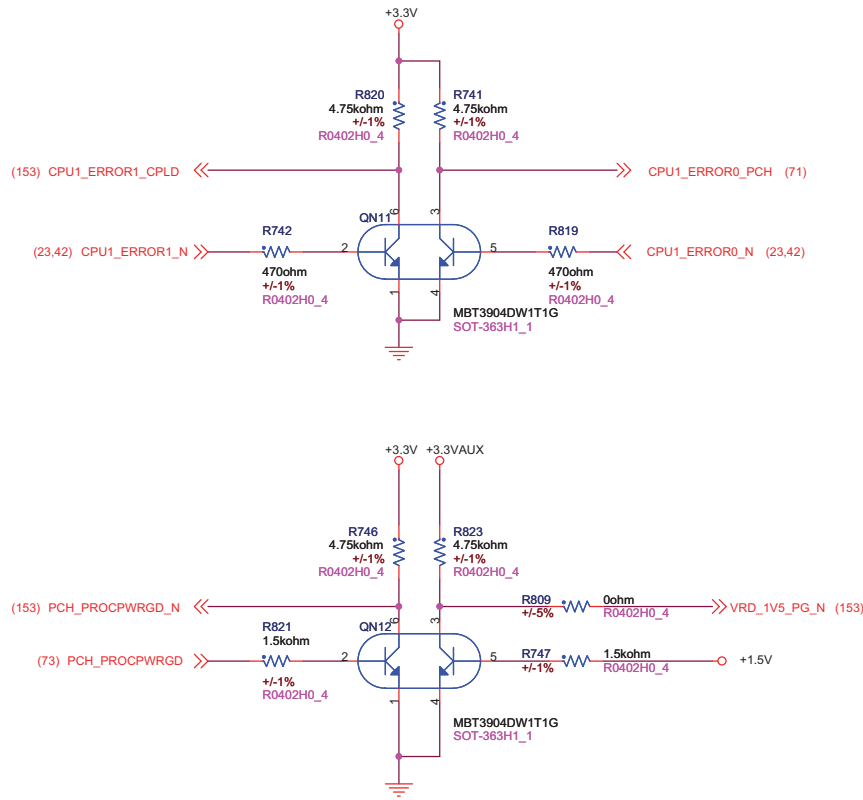
Personal Computer & Enterprise
Business Group (PCEBG)
Module Integration Business Group (MIBG)

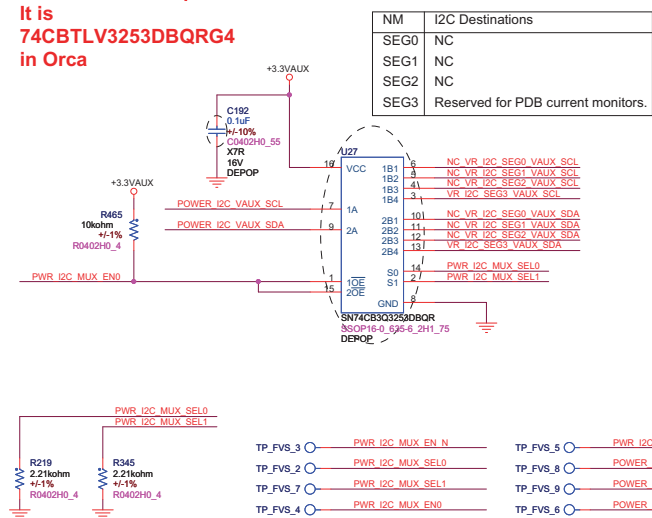
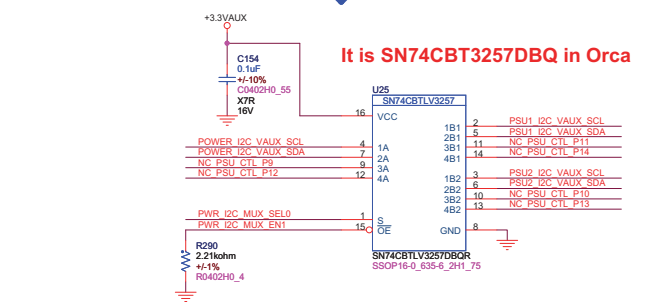
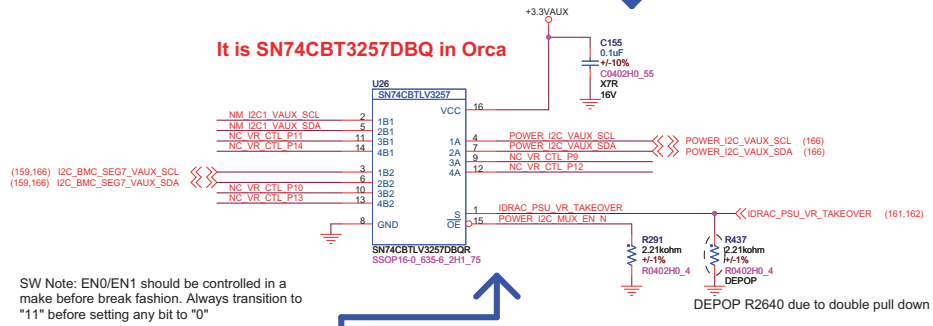
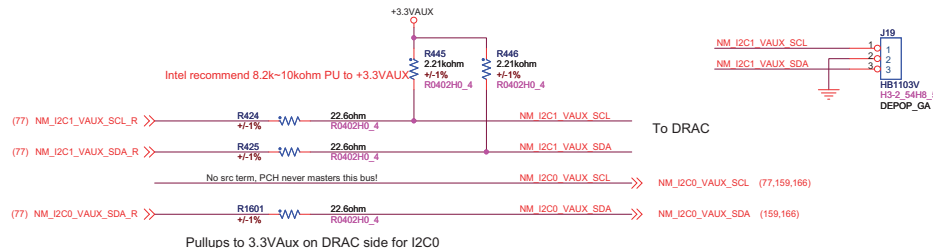
Hon Hai Precision Ind. Co., Ltd.

Title
PCH PU/PD

Document Number: PCB P/N: 01015C800-000-G	Sheet 84 of 185	Rev X00
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01/25/2011, 10:57 AM



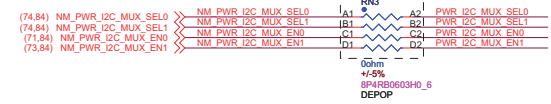


TP_FVS_3	PWR_I2C_MUX_EN_N	TP_FVS_5	PWR_I2C_MUX_EN1
TP_FVS_2	PWR_I2C_MUX_SEL0	TP_FVS_6	POWER_I2C_VAUX_SCL
TP_FVS_7	PWR_I2C_MUX_SEL1	TP_FVS_9	POWER_I2C_VAUX_SDA
TP_FVS_4	PWR_I2C_MUX_EN0	TP_FVS_6	POWER_I2C_MUX_EN_N

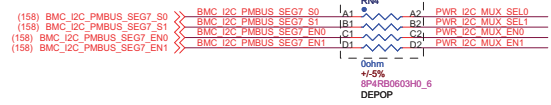
<http://adf.ly/3o8pJ>

PMBus Control Signal Control Population Options (Pick ONE)

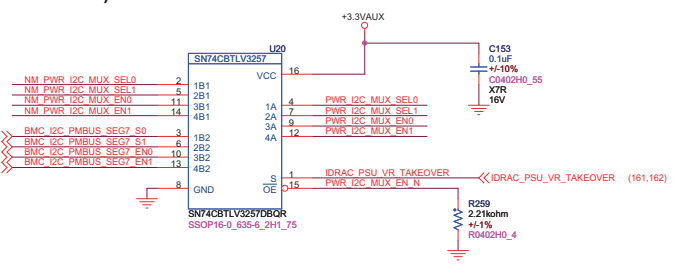
NM Direct Control (RTS POR)



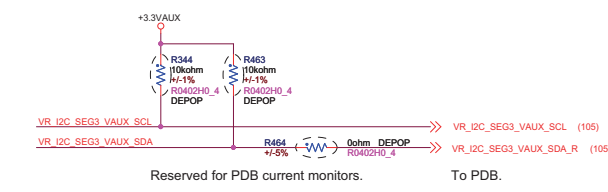
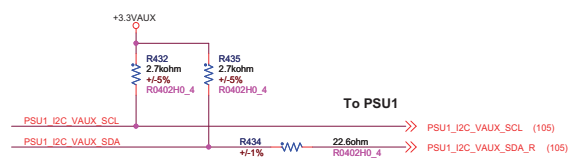
DRAC Direct Control (NM Backout)



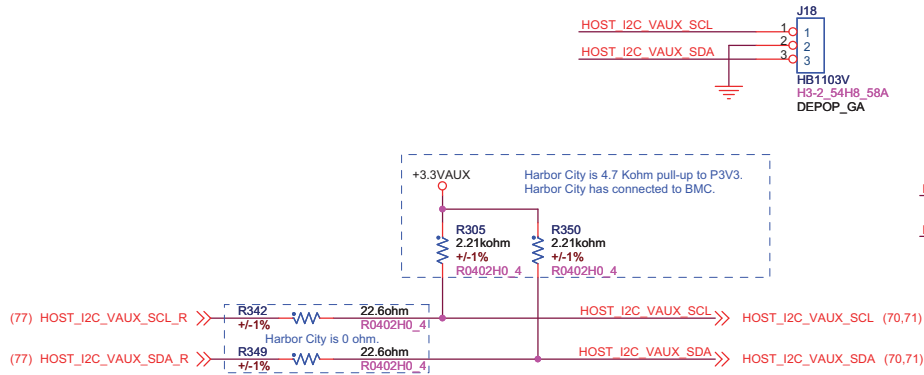
DRAC Takeover (BU/Pre-ME FW)



PSU Segments



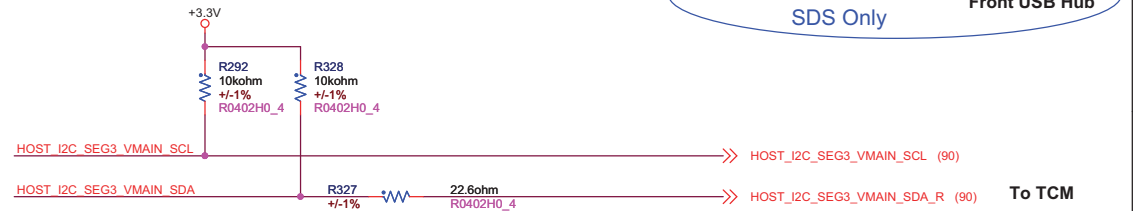
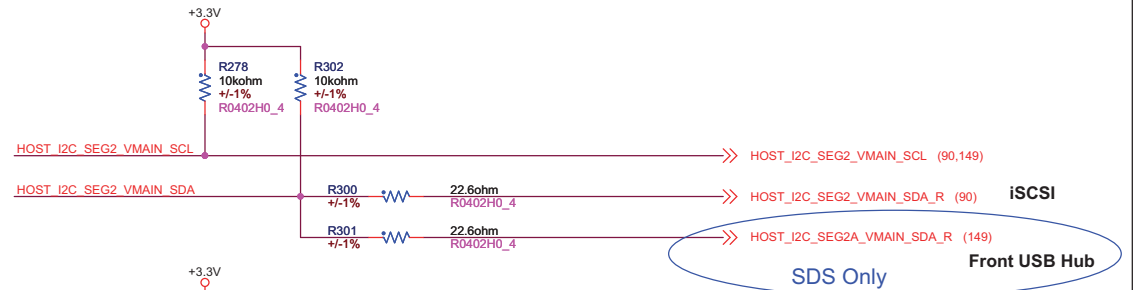
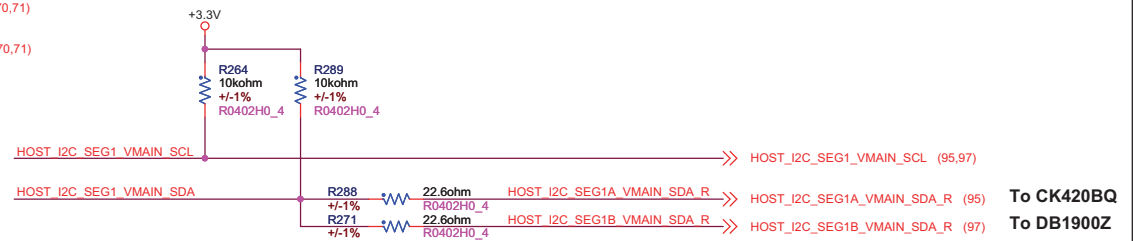
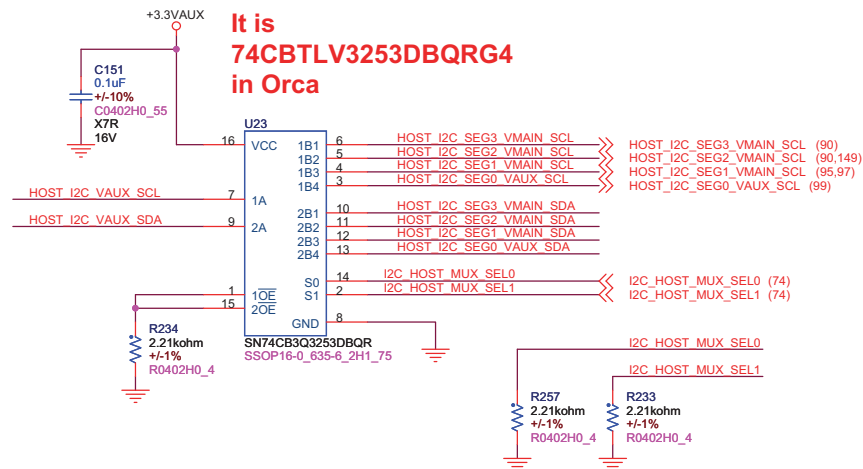
Host I2C Page



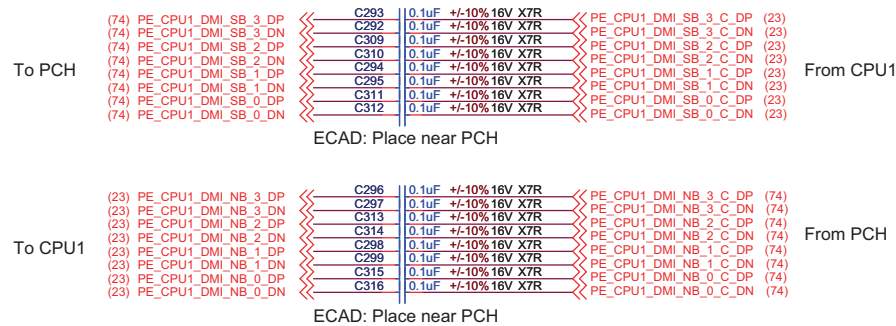
Different description from Orca

HOST	I2C Destinations
SEG0	CKMNG+
SEG1	CK420BQ, CK1900Z
SEG2	iSCSI
SEG3	Security PIM

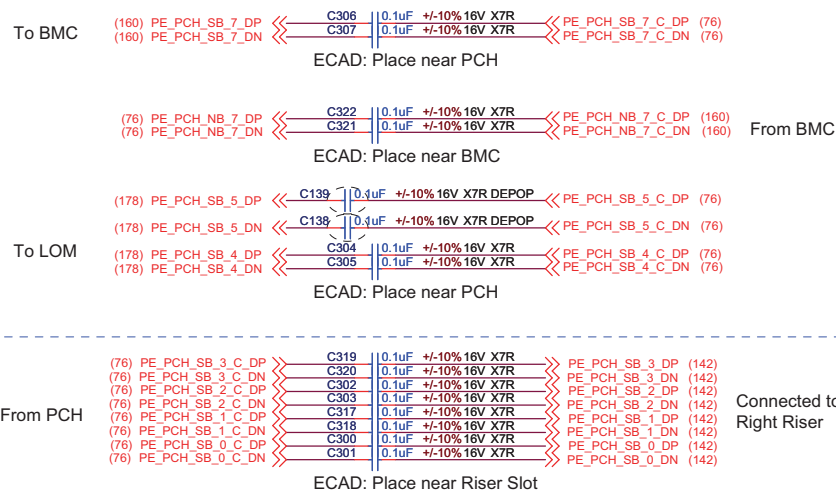
It is
74CBTLV3253DBQRG4
in Orca



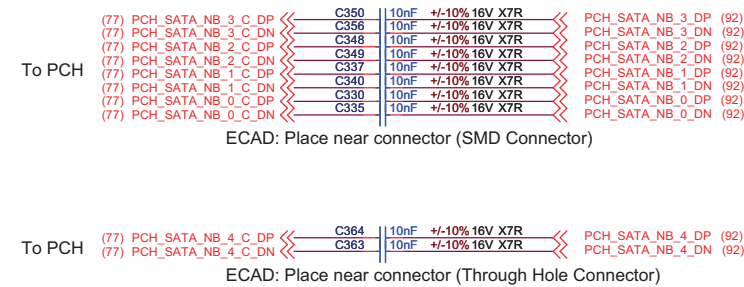
DMI AC Caps



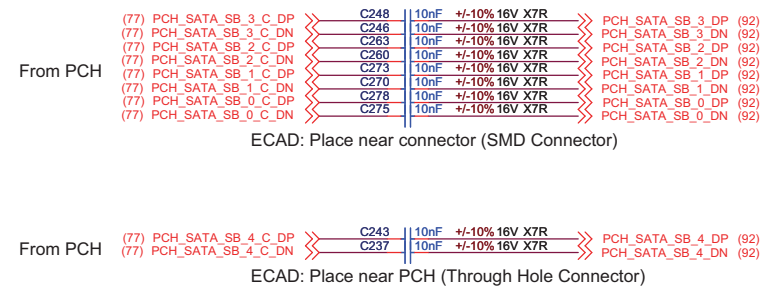
PCIe AC Caps

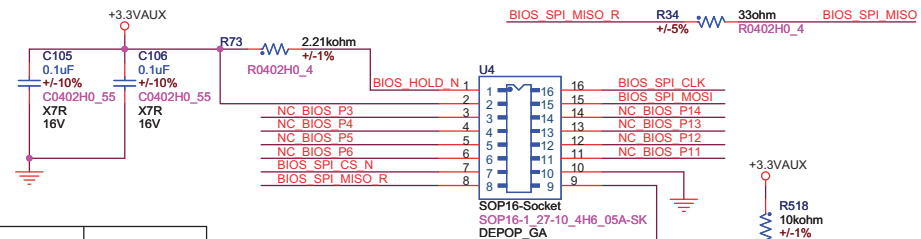
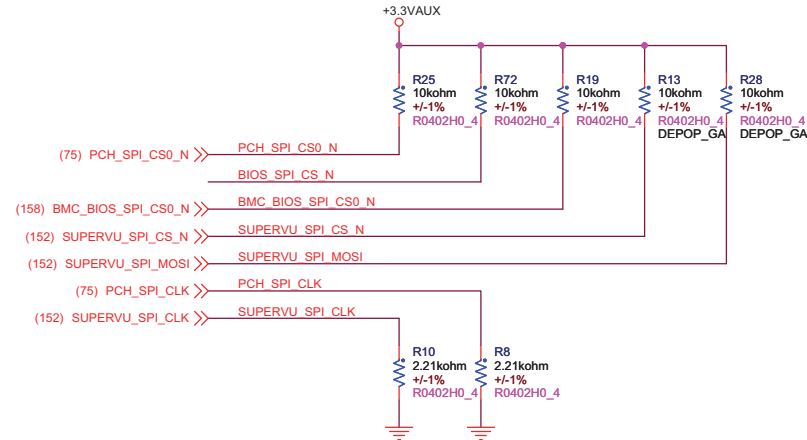
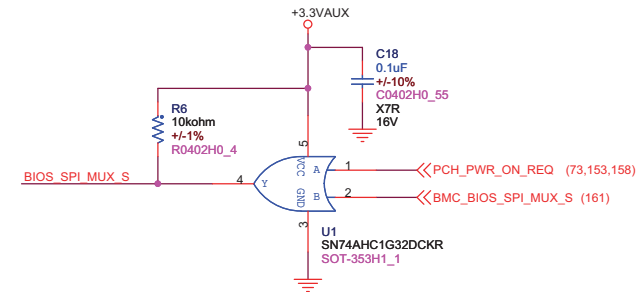
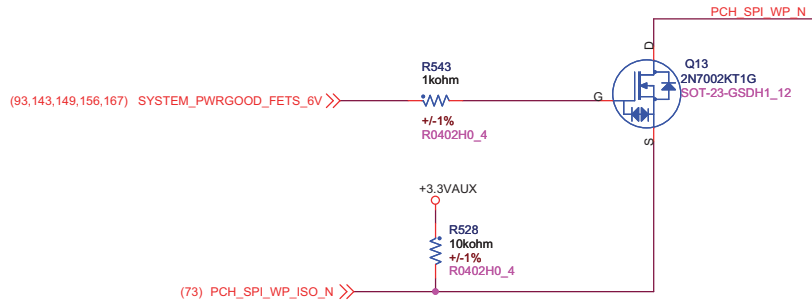
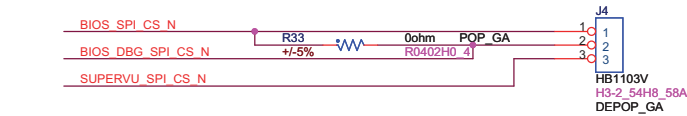
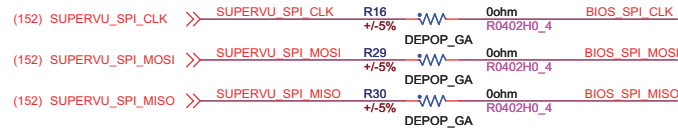
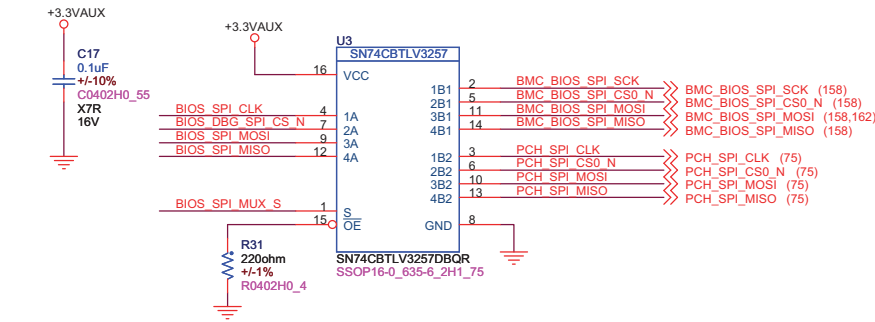


SATA AC Caps (NB)



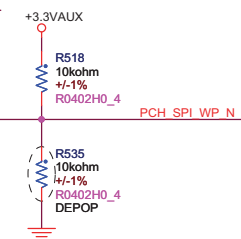
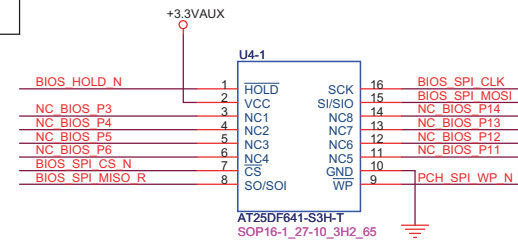
SATA AC Caps (SB)

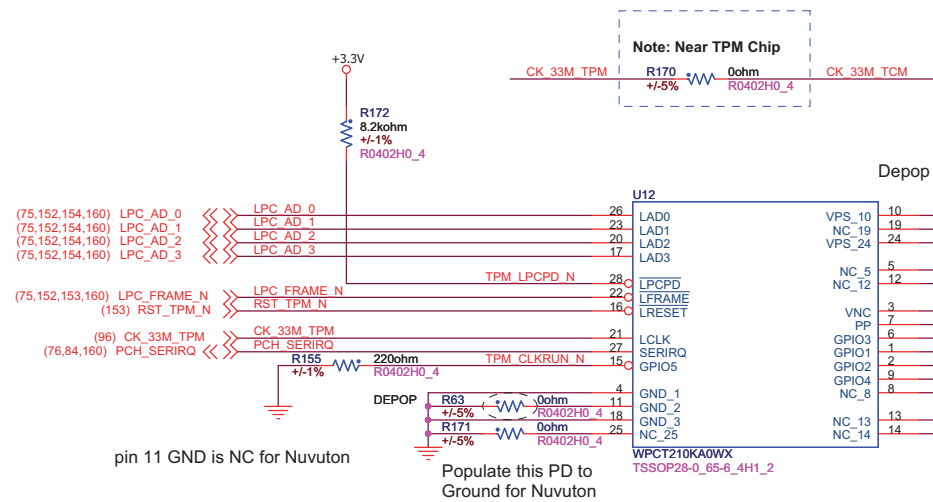




IC, PROG	5119G
BLANK PART	231W1
DSK, PROG	HGRR1

Same as Orca??





Bring-Up modum: Depopulate TPM since BIOS is not supporting before UT. Strapping is for STmicro for Bringup board for now

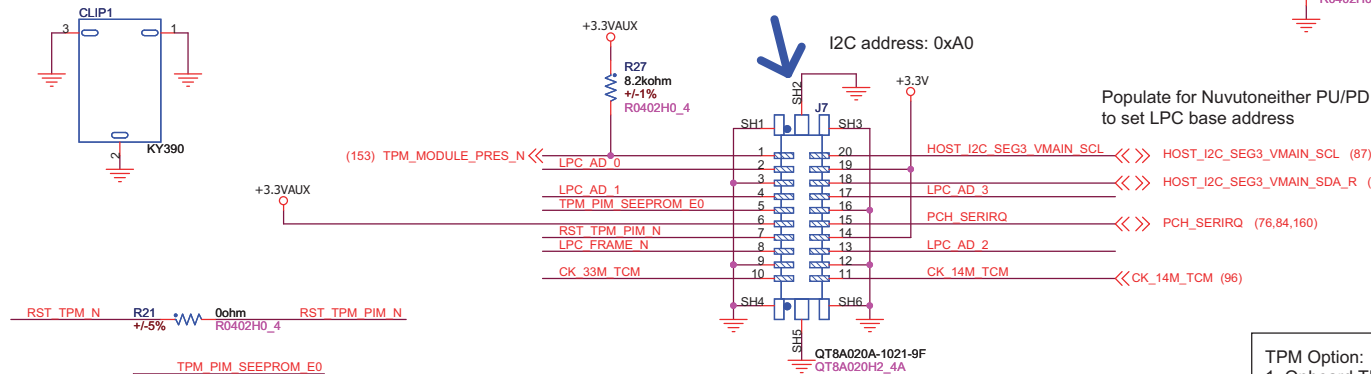
UnitTest modum: Use P295K (Current Nuvuton)

PT build and beyond should be using PT659 (Nuvuton NPCT420JA0WX EK cert with TCG116), available Jan2011

Previous plan on ProductTest modum & later: (was going to use 75TFW (NPCT410J with EK cert TCG103 avail early November 2010)

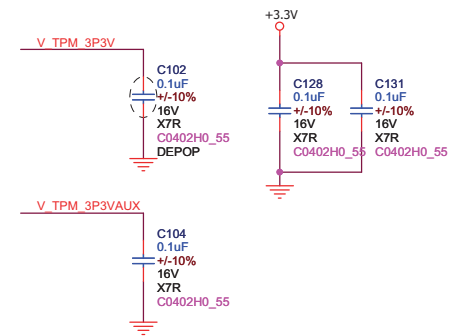
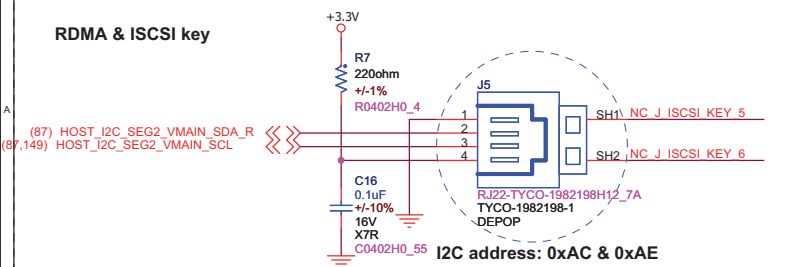
ECAD: place within 1000mils

I2C address: 0xA0

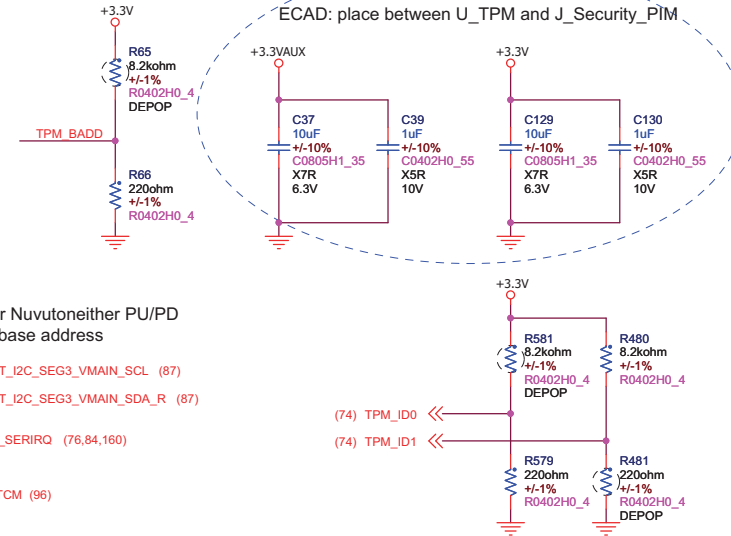


Security PIM (Plug In Module) header

RDMA & ISCSI key



ECAD: place between U_TPM and J_Security_PIM

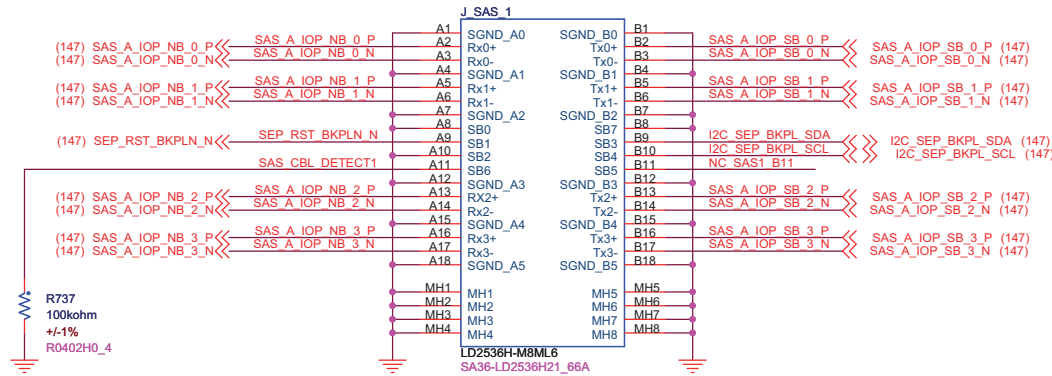


TPM Option:

1. Onboard TPM Installed (Nuvuton)
2. TPM PIM Connector installed (no onboard TPM), and PIM installed
3. TPM PIM Connector installed (no onboard TPM), and no PIM installed

TPM_ID1	TPM_ID0	Description
0	0	PIM (Daughter card, check PIM presence bit)
0	1	STMicro
1	0	Nuvuton (ROW)
1	1	Reserved

Mini SAS Internal Connector (PORT A)



Mini SAS Internal Connector (PORT B)

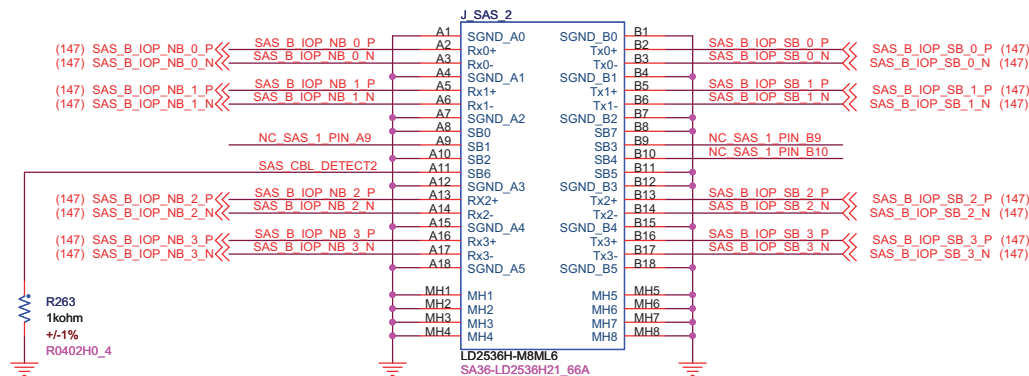


Table 10 — Controller Mini SAS 4i connector pin assignments and physical link usage

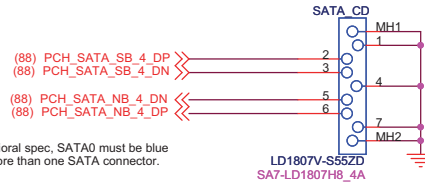
Signal	Pin usage based on number of physical links supported by the cable assembly ^a				Mating level ^b
	One	Two	Three	Four	
Rx 0+	A2	A2	A2	A2	Third
Rx 0-	A3	A3	A3	A3	
Rx 1+	N/C	A5	A5	A5	
Rx 1-	N/C	A6	A6	A6	First
Sideband 7	A8	A8	A8	A8	
Sideband 3	A9	A9	A9	A9	
Sideband 4	A10	A10	A10	A10	Third
Sideband 5	A11	A11	A11	A11	
Rx 2+	N/C	N/C	A13	A13	
Rx 2-	N/C	N/C	A14	A14	Third
Rx 3+	N/C	N/C	N/C	A16	
Rx 3-	N/C	N/C	N/C	A17	
Tx 0+	B2	B2	B2	B2	Third
Tx 0-	B3	B3	B3	B3	
Tx 1+	N/C	B5	B5	B5	
Tx 1-	N/C	B6	B6	B6	First
Sideband 0	B8	B8	B8	B8	
Sideband 1	B9	B9	B9	B9	
Sideband 2	B10	B10	B10	B10	Third
Sideband 6	B11	B11	B11	B11	
Tx 2+	N/C	N/C	B13	B13	
Tx 2-	N/C	N/C	B14	B14	Third
Tx 3+	N/C	N/C	N/C	B16	
Tx 3-	N/C	N/C	N/C	B17	
SIGNAL GROUND	A1, A4, A7, A12, A15, A18, B1, B4, B7, B12, B15, B18				First

^a N/C = not connected

^b The mating level indicates the physical dimension of the contact (see SFF-8086).

CDROM Connectors

SATA PORT 0

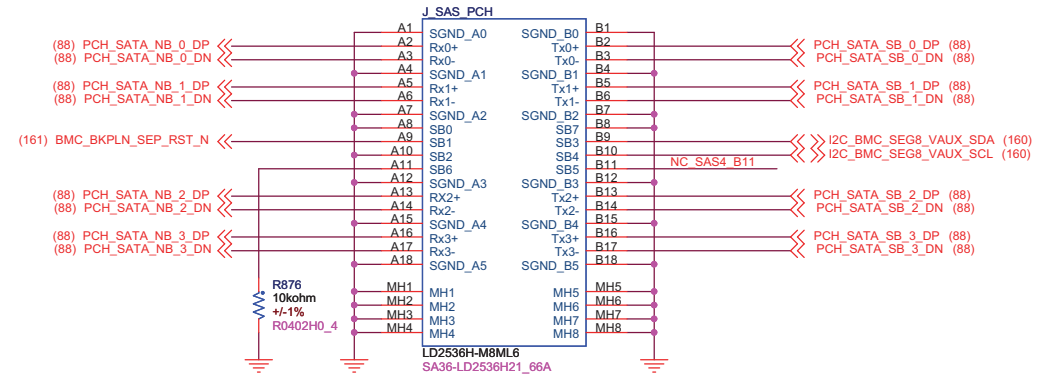


Due to a broken behavioral spec, SATA0 must be blue if any only if there is more than one SATA connector. Else it must be black.

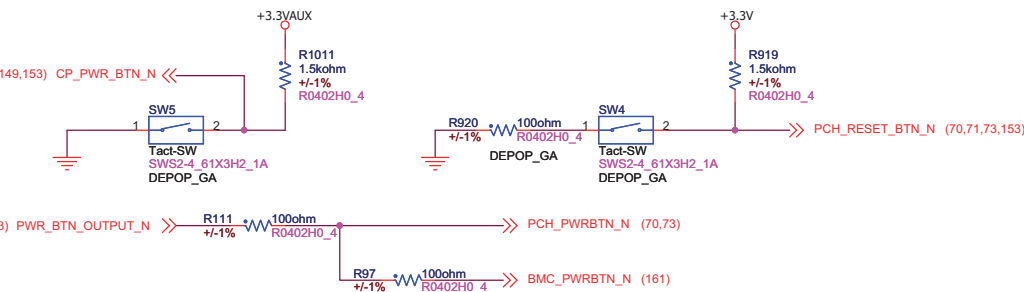
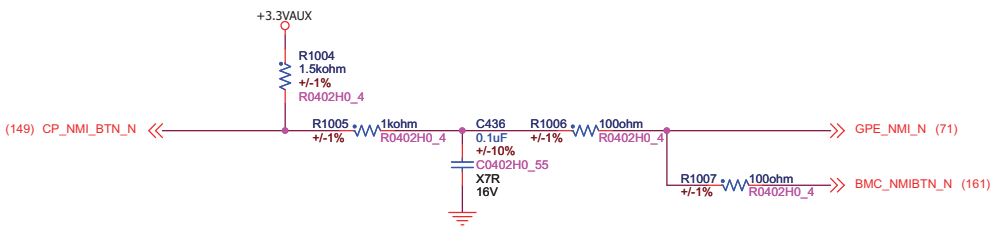
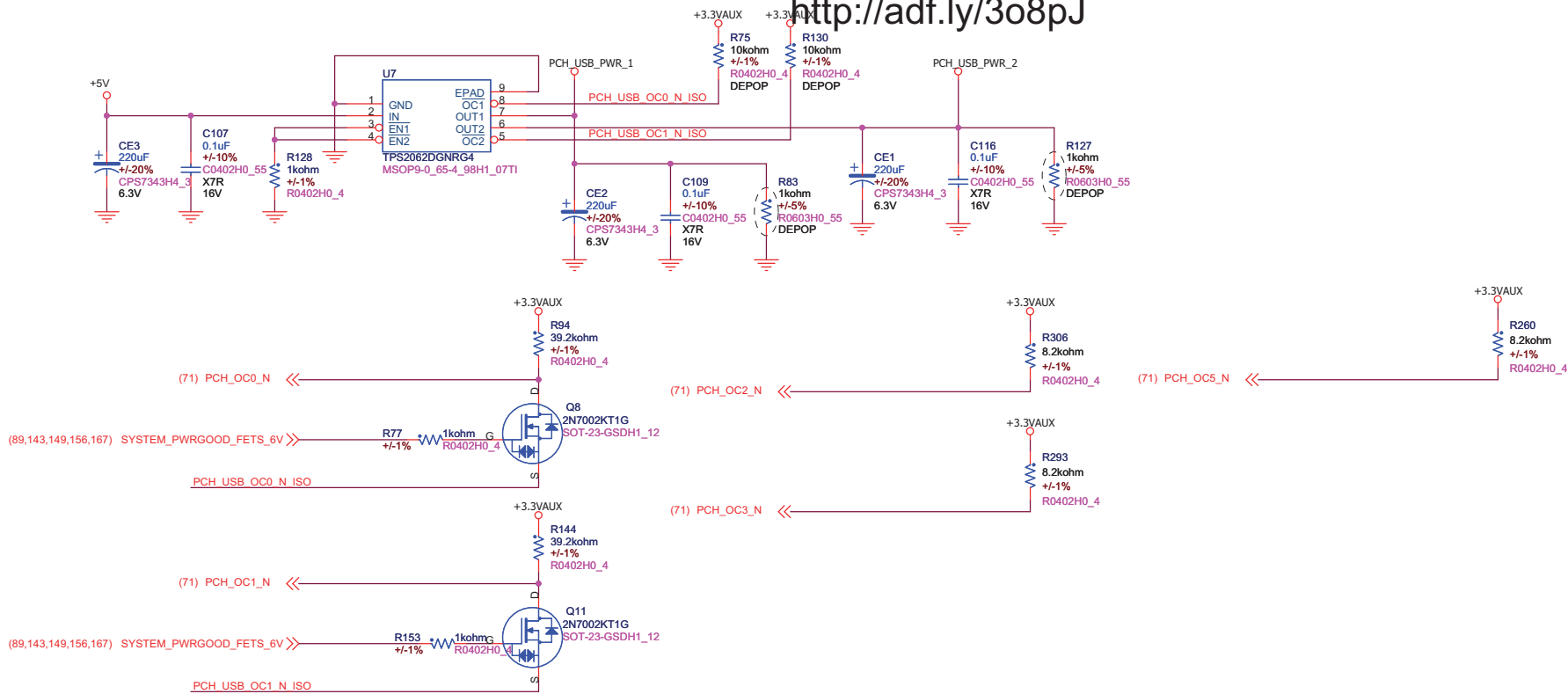
Color: Blue

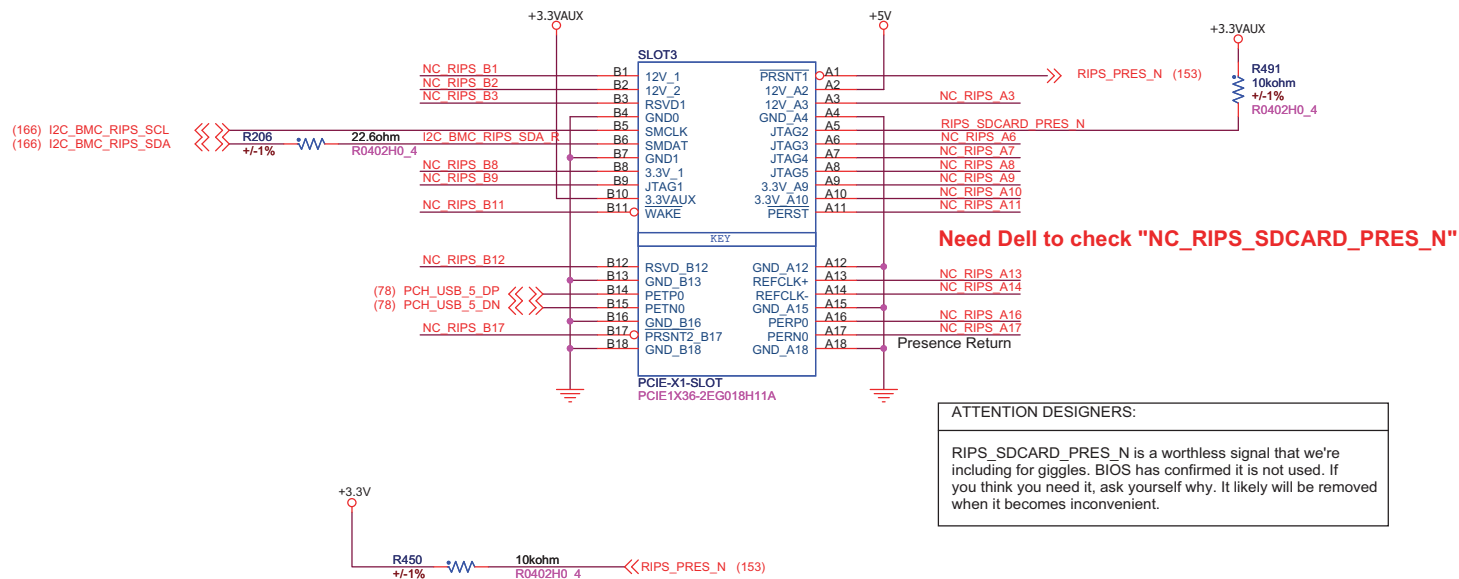
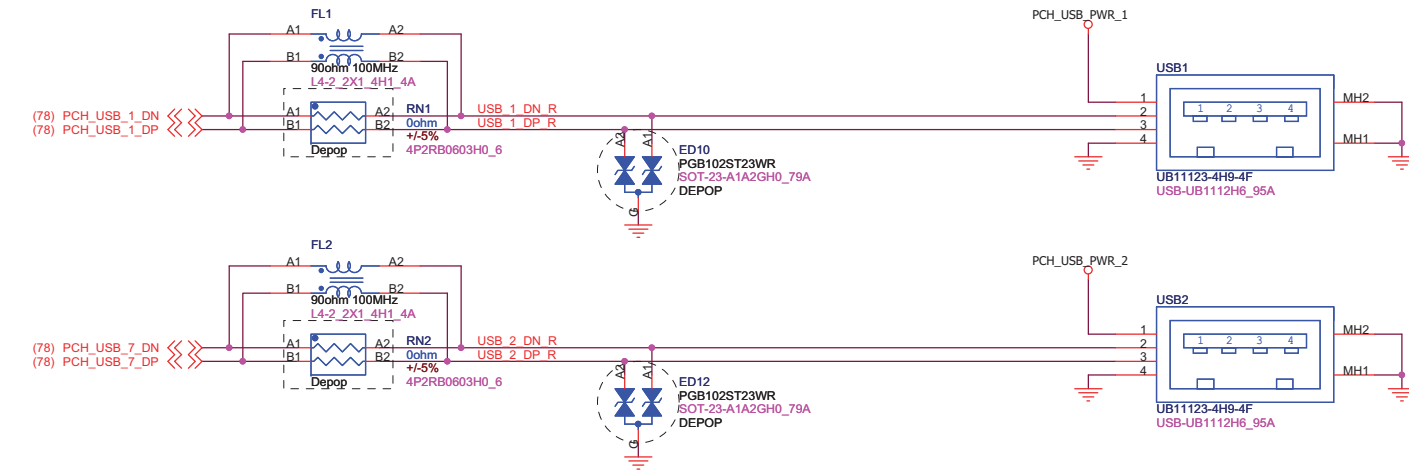


SAS Connectors



<http://adf.ly/3o8pJ>





Note: Disable un-used clock by BIOS

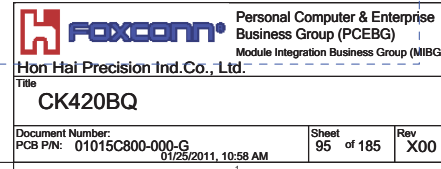
VDD Plane Filtering



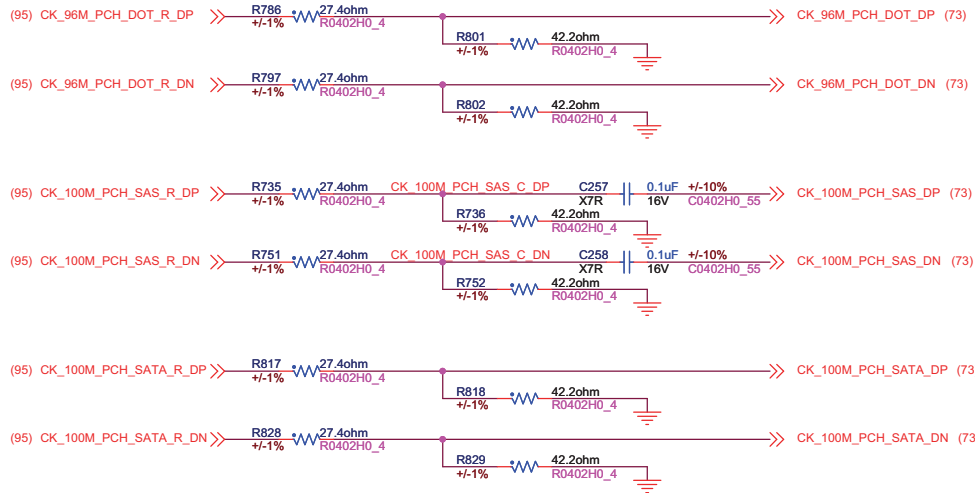
- Do not split the 2 halves of a diff clk pair between layers. Route clks to agents on the same physical routing layer.
- Route clks to all Intel QPI agents (Sandy Bridge) on the same physical layer. (after Source-Shunt termination)
- Route clks to the PCH on the same physical layer.
- Clk traces should not cross any plane splits on adjacent layers.
- Layer transition for reference clk routing not allowed for normal topologies, unless it is for the Source-Shunt Termination Placement or for breaking out the sig at the receiver
- All clocks going to the CPU (QPI clk and PCIe ref clk) must be matched within 0.5 in pin-pin.
- The ground flood should be via'd through the ground plane with no less than 12 to 16 vias under the part.
- The DB1900Z external board feedback trace must be routed on the outer layer and should be as short as possible < 680 mils. Match prop dly as close as possible to 125ps.

Notes

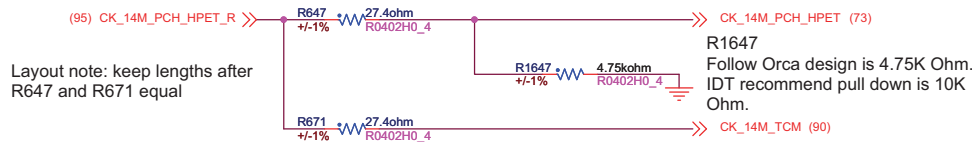
- PCH and TPM have to share the same 33Mhz clock for security reasons
- BIOS: Stop unused output clocks (all NC_CK_*).



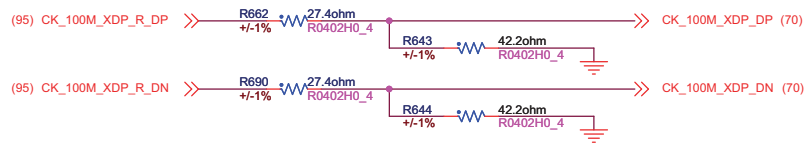
PCH Storage Clocks



PCH and TCM Shared Clock



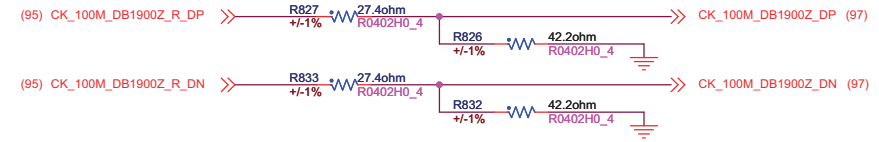
XDP Clock



CPLD Clock



DB1900Z Clock Buffer



SPIVU2 Clocks



BMC LPC Clocks



PCH Clock

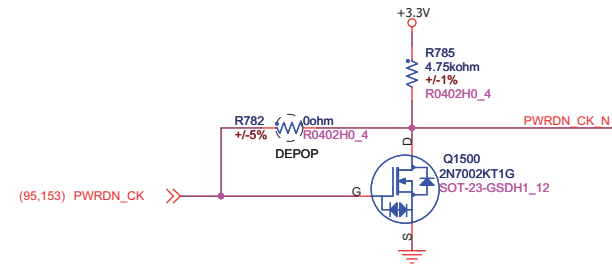
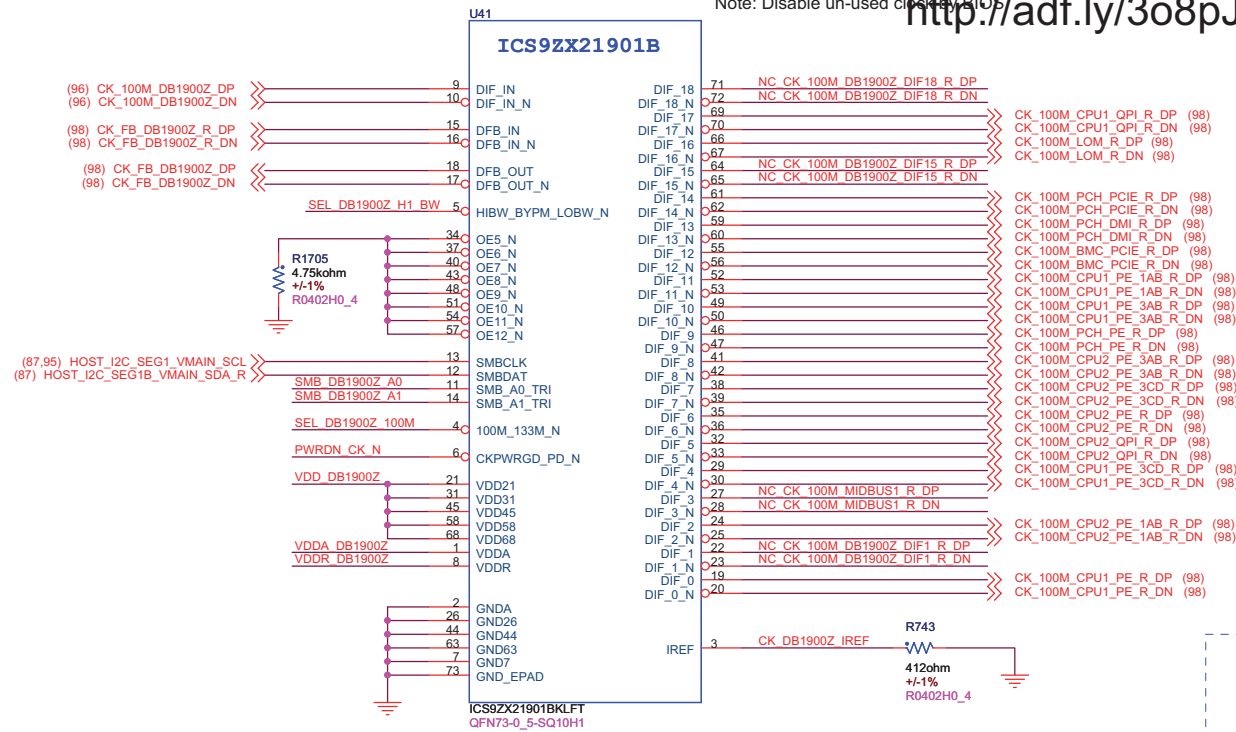


TPM Clock



Note: Disable un-used clocks by BIOS

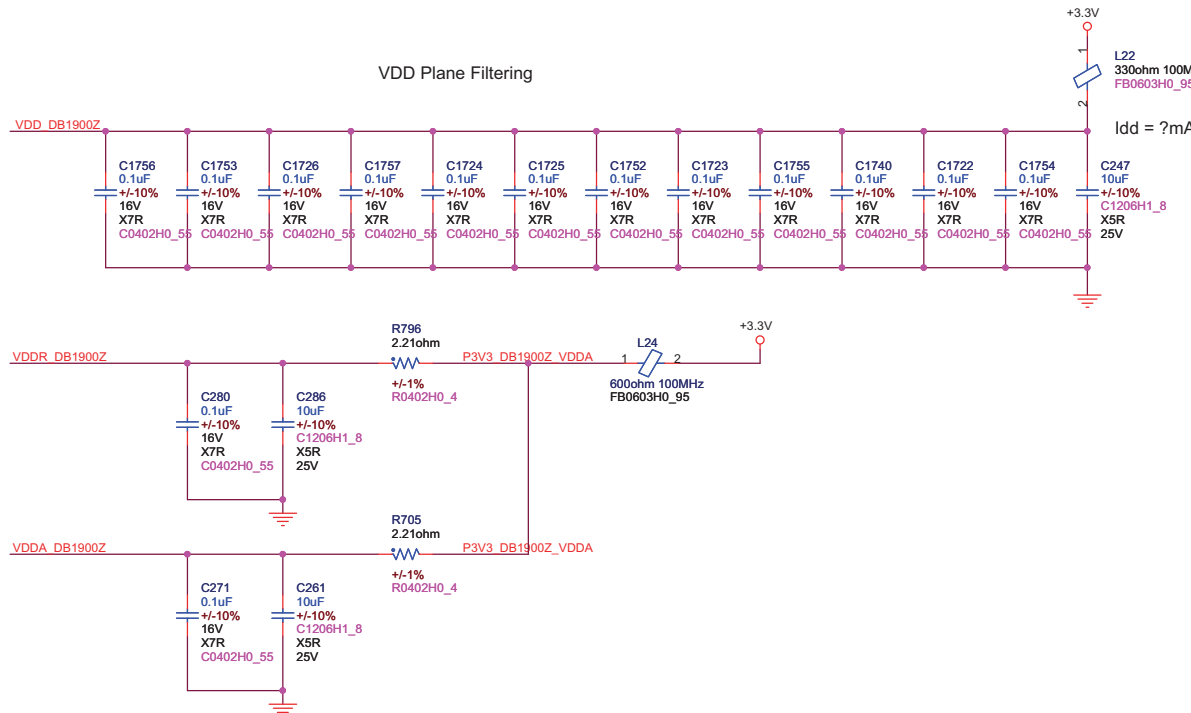
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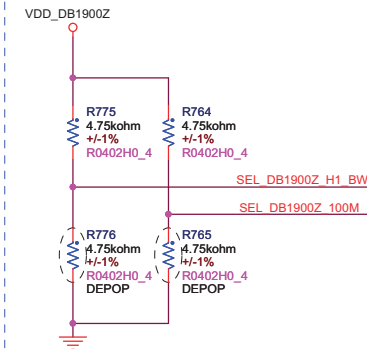
PCIE Midbus Debug Clocks

Not supported in GR

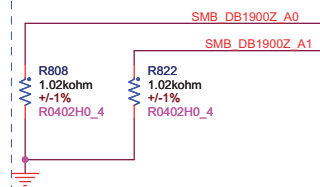
VDD Plane Filtering



Operating Freq and Bandwidth Select



I2C Addr

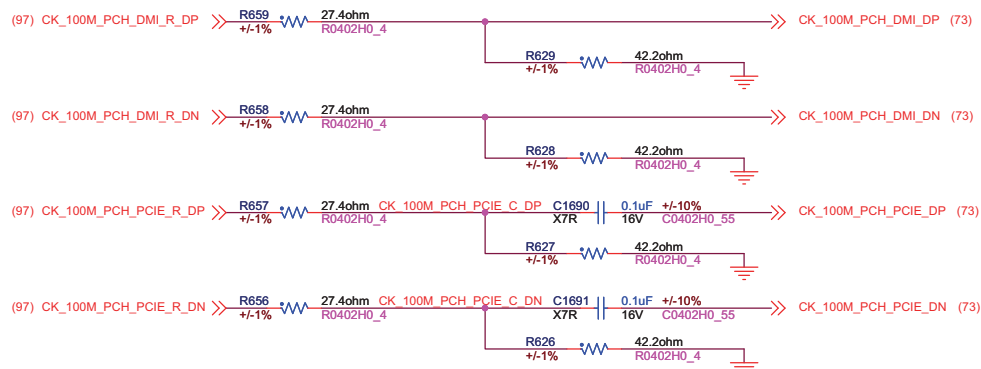


SMBus Address Table

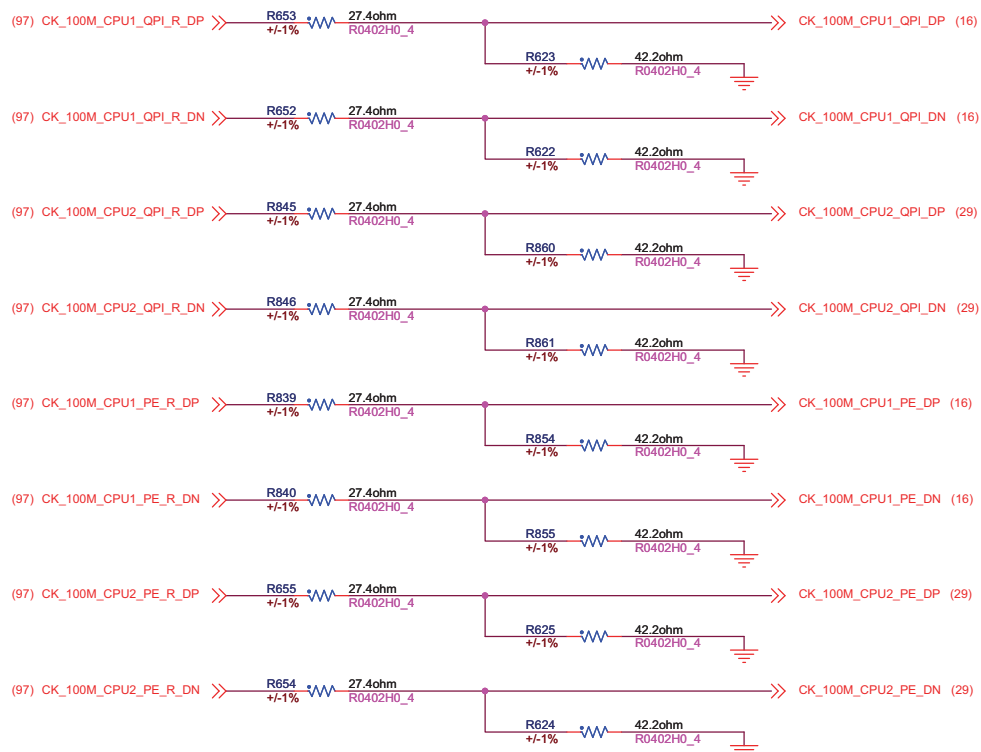
SA_1	SA_0	SMBus Address
L	L	D8

http://adf.ly/3o8pJ

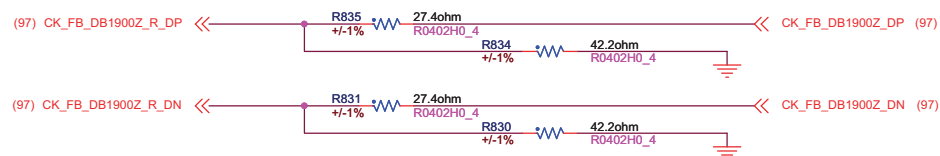
PCH Clocks



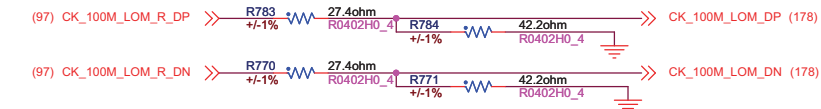
CPU Clocks



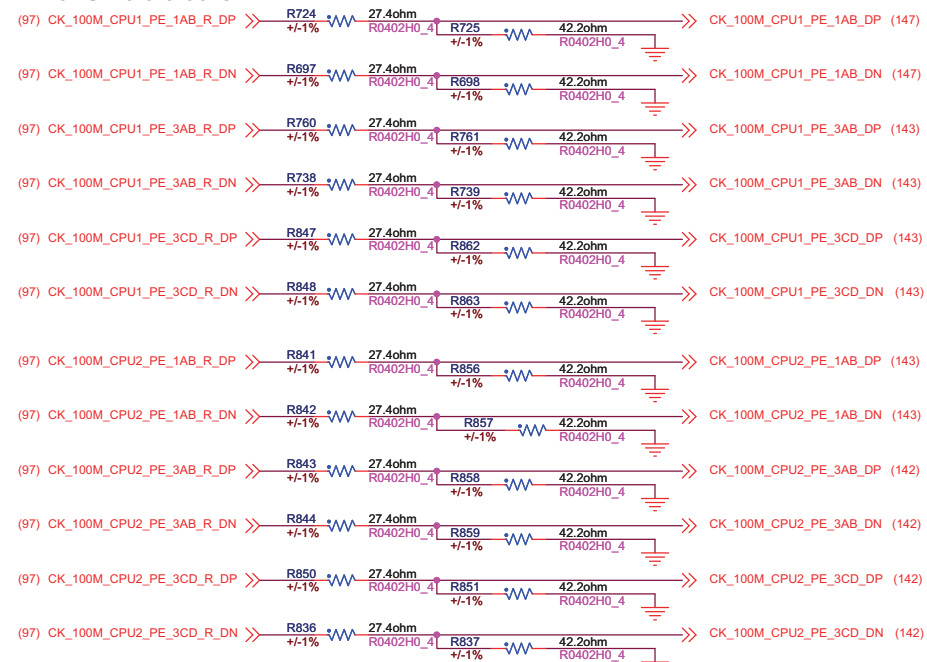
Feedback Clocks



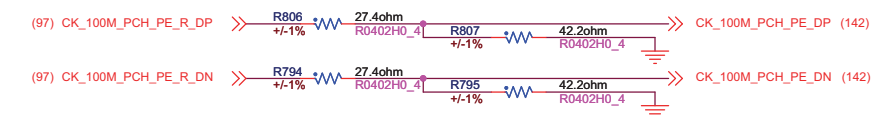
LOM Clocks



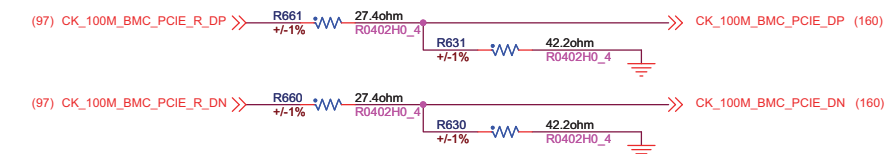
CPU PCIe Clocks

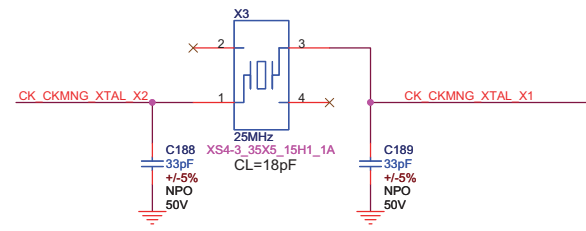
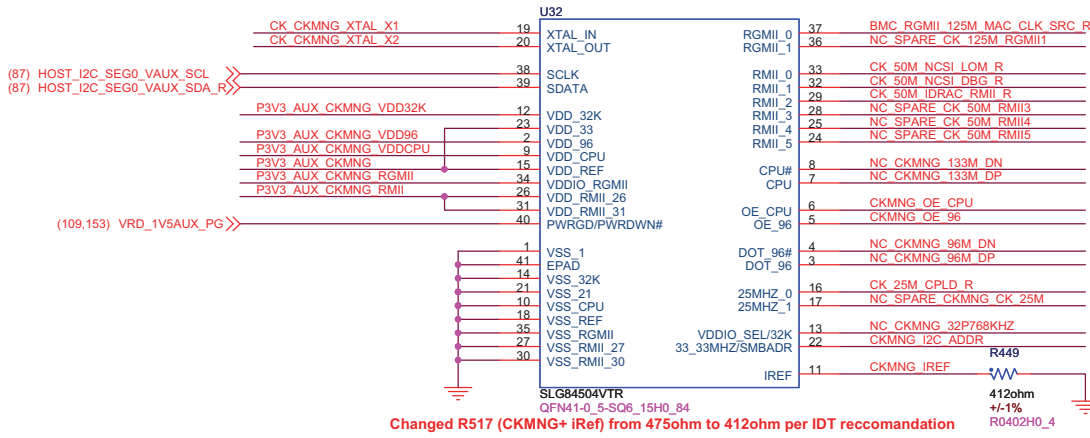


PCH PCIe Clocks

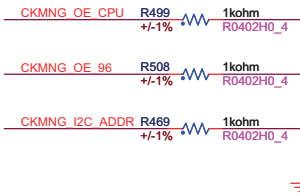
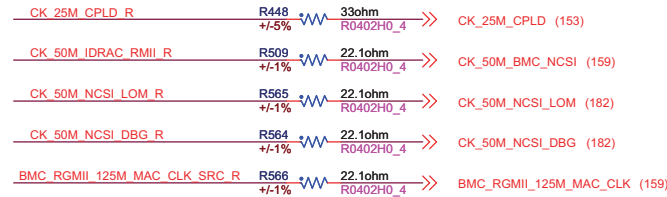


iBMC Clock





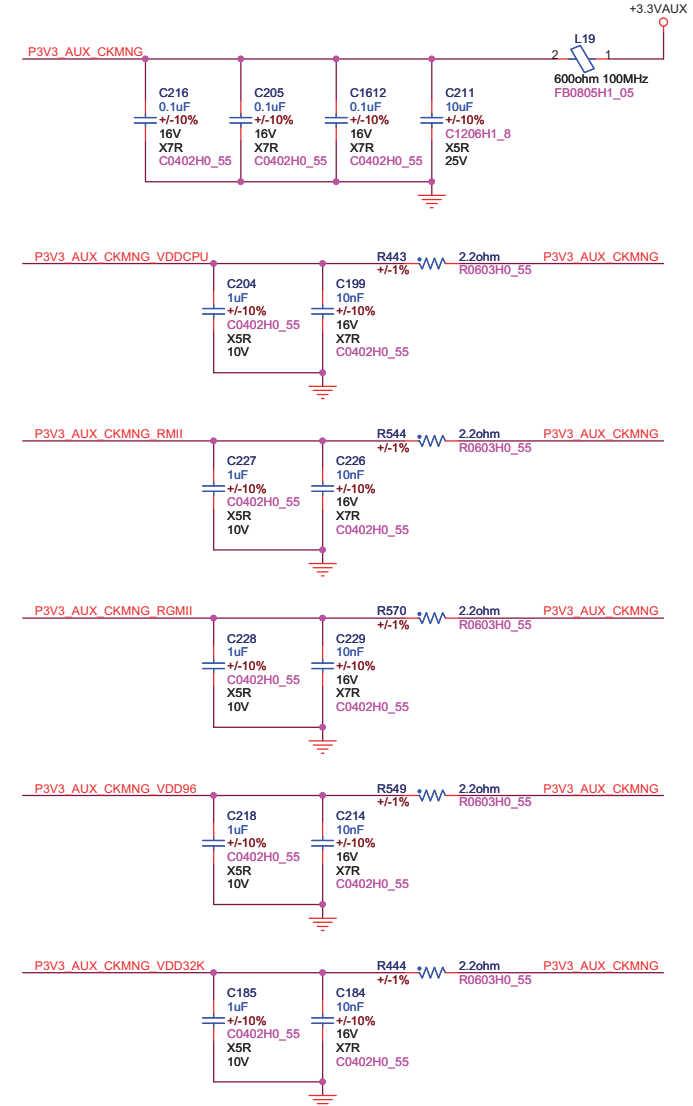
Clocks



OE_CPU	IN	Active high input for enabling CPU DIFF pairs. 1 = enable output(s), 0 = tri-state output(s)
OE_96	IN	Active high input for enabling 96Hz outputs. 1 = enable output(s), 0 = tri-state output(s)

SMBus Address Selection	
SMBADR	
*SMBADR = 0	SMBADR = 1
D0/D1	C0/C1
* Default value	

VDD Plane Filtering



Notes

- This is a Dell custom part. No price increase from the regular CKMNG+.
- Pin 33 (50MHz), Pin 32(50MHz), Pin 29(50MHz) and Pin 16 (25MHz) go active before VTTTPWR_GD (Pin 40) goes high.

FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)
Hon Hai Precision Ind. Co., Ltd.

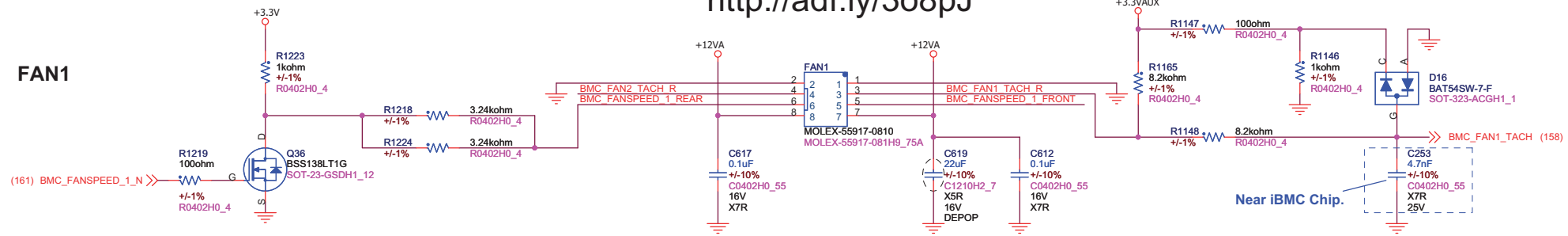
Title: **CKMNG+**

Document Number: 01015C800-000-G
PCB P/N: 01015C800-000-G
01/25/2011, 10:57 AM

Sheet 99 of 185
Rev X00

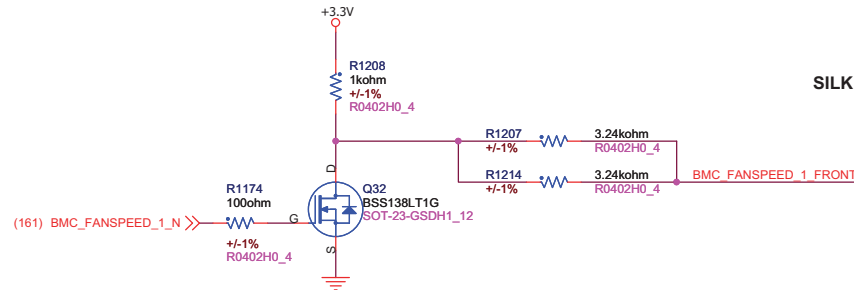
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FAN1

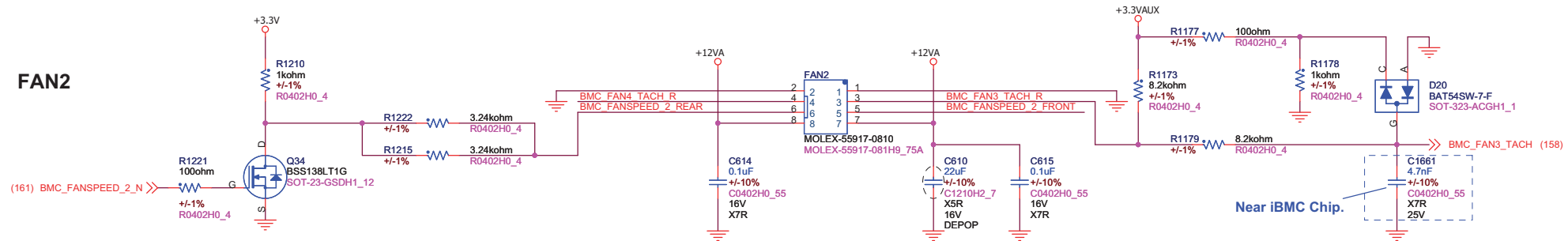


FAN's Power Trace width must \geq 50 mils.

SILK will use One FAN Speed and Tach from this Connector.

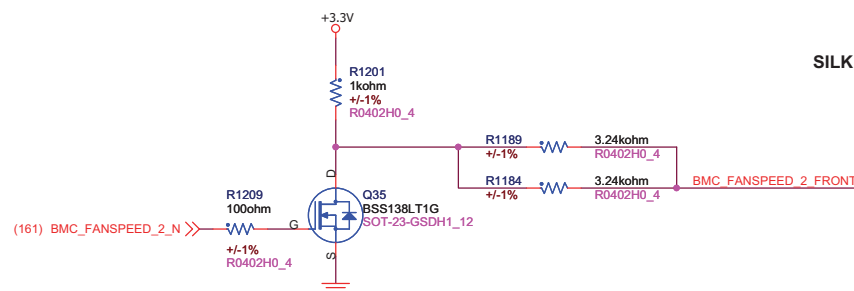


FAN2



FAN's Power Trace width must \geq 50 mils.

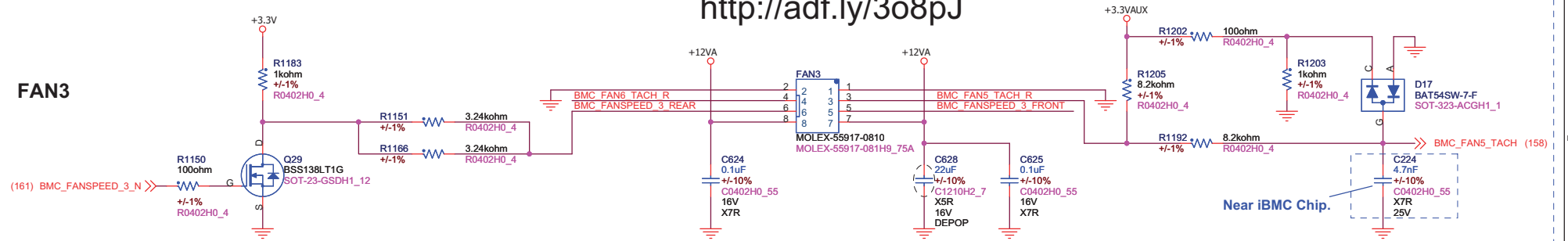
SILK will use One FAN Speed and Tach from this Connector.



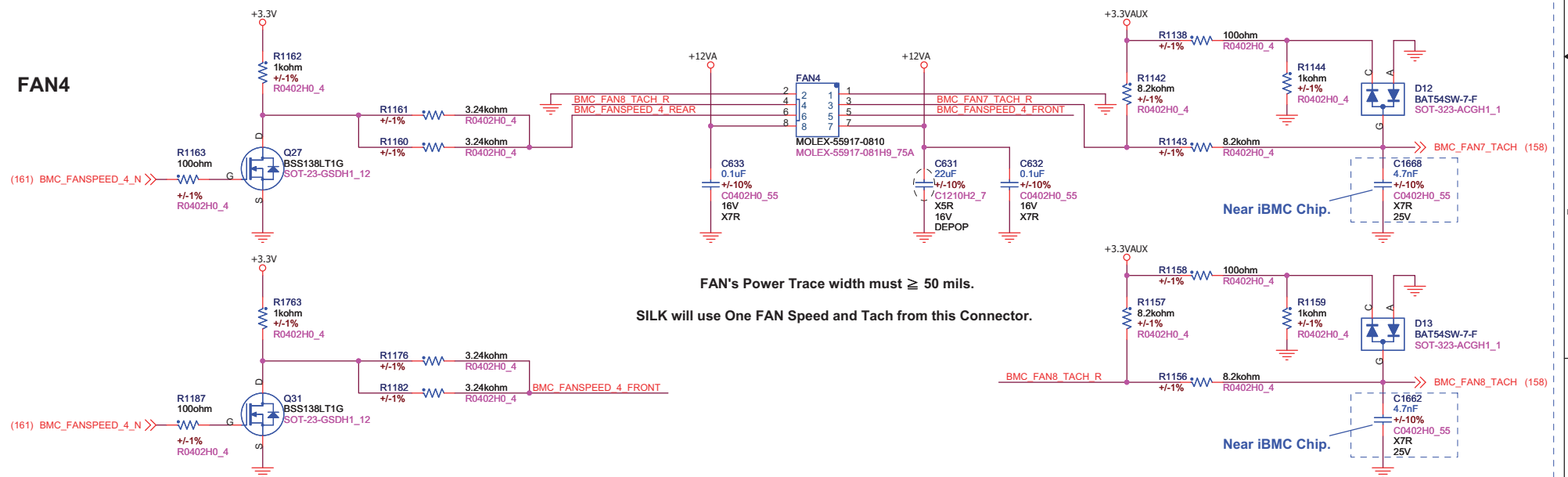
Design Note:

Some fan failure cases have various signal pins shorted to 12volts. If the fanspeed signal is shorted to 12V, these two resistors limit the current preventing damage to the FET. Two 0402 parts are needed for power dissipation.

FAN3



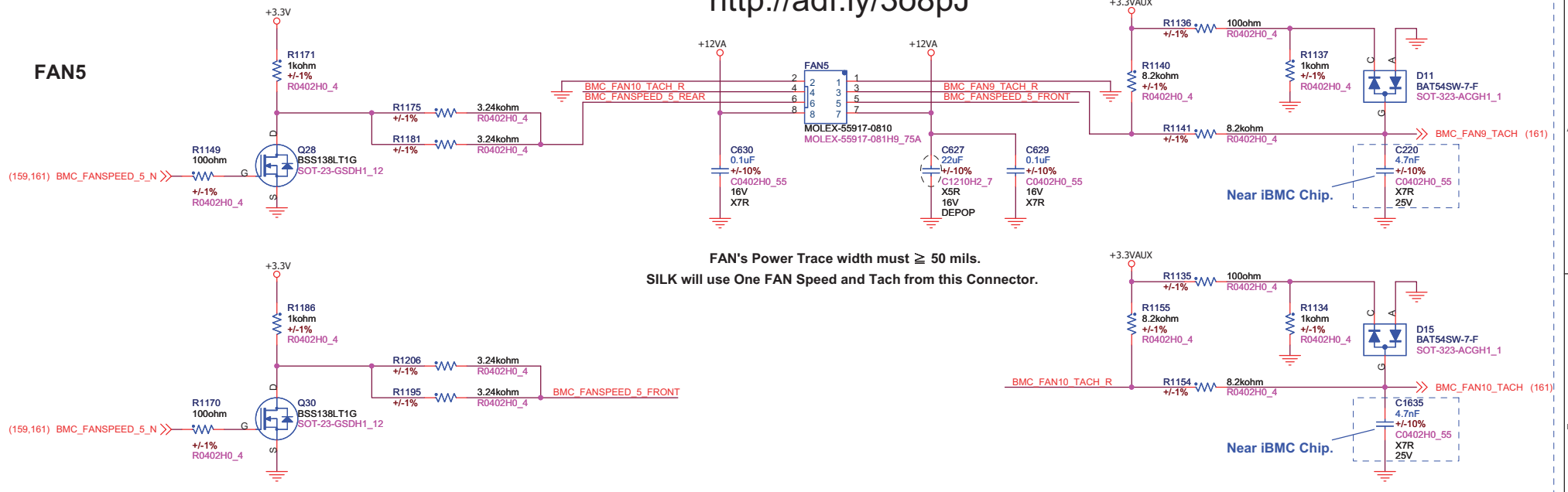
FAN4



Design Note:
Some fan failure cases have various signal pins shorted to 12volts. If the fanspeed signal is shorted to 12V, these two resistors limit the current preventing damage to the FET. Two 0402 parts are needed for power dissipation.

<http://adf.ly/3o8pJ>

FAN5



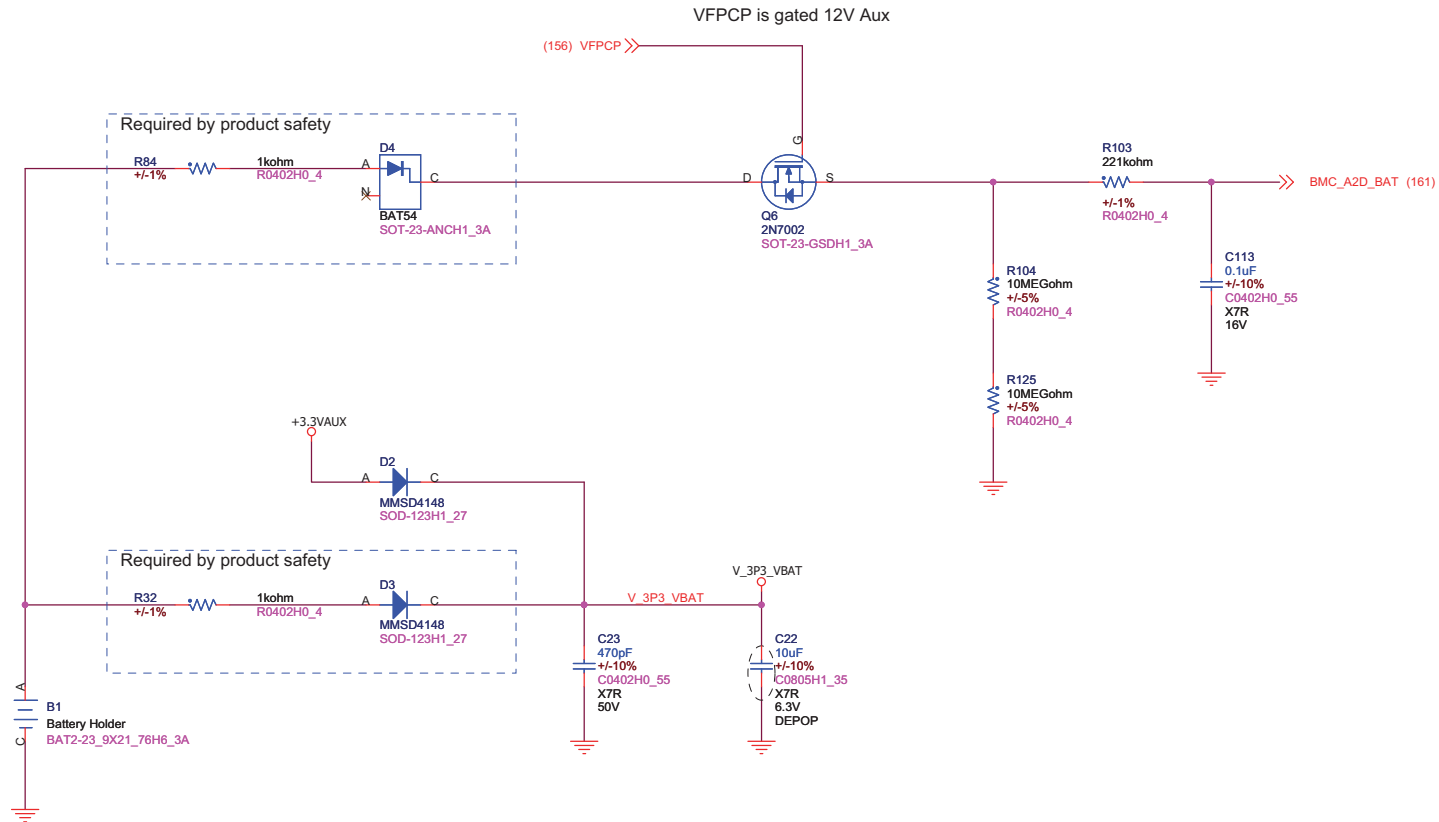
FAN's Power Trace width must ≥ 50 mils.
SILK will use One FAN Speed and Tach from this Connector.

Design Note:
Some fan failure cases have various signal pins shorted to 12volts. If the fanspeed signal is shorted to 12V, these two resistors limit the current preventing damage to the FET. Two 0402 parts are needed for power dissipation.

BATTERY

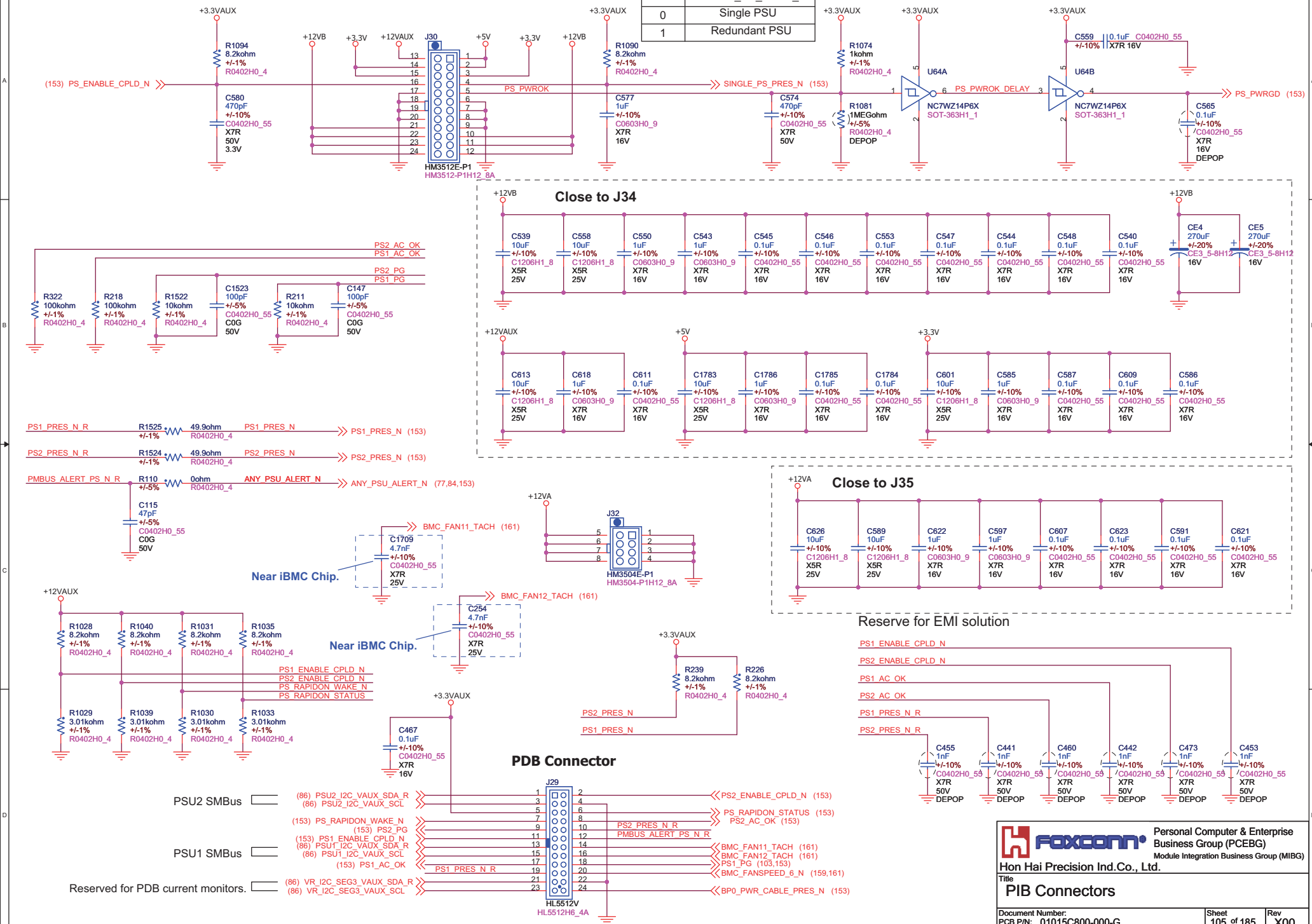


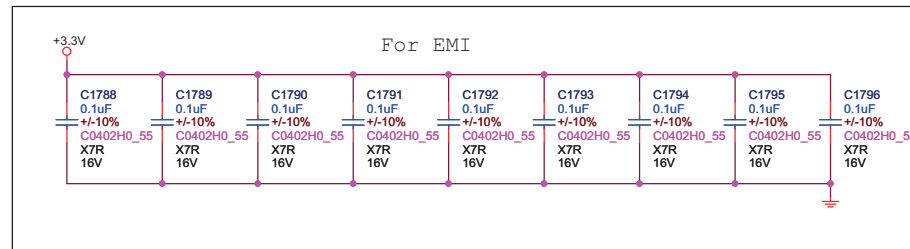
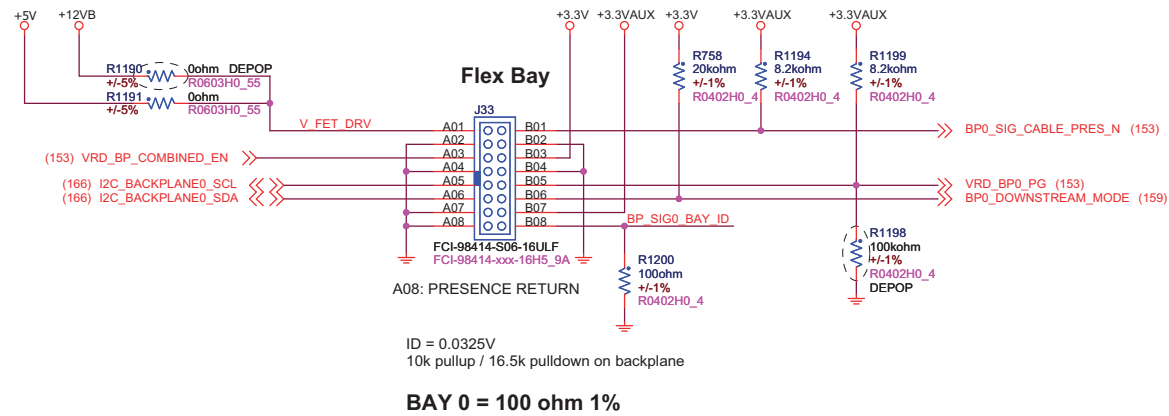
Battery CR-2032L/BE



ord/pidfont/3o8p...

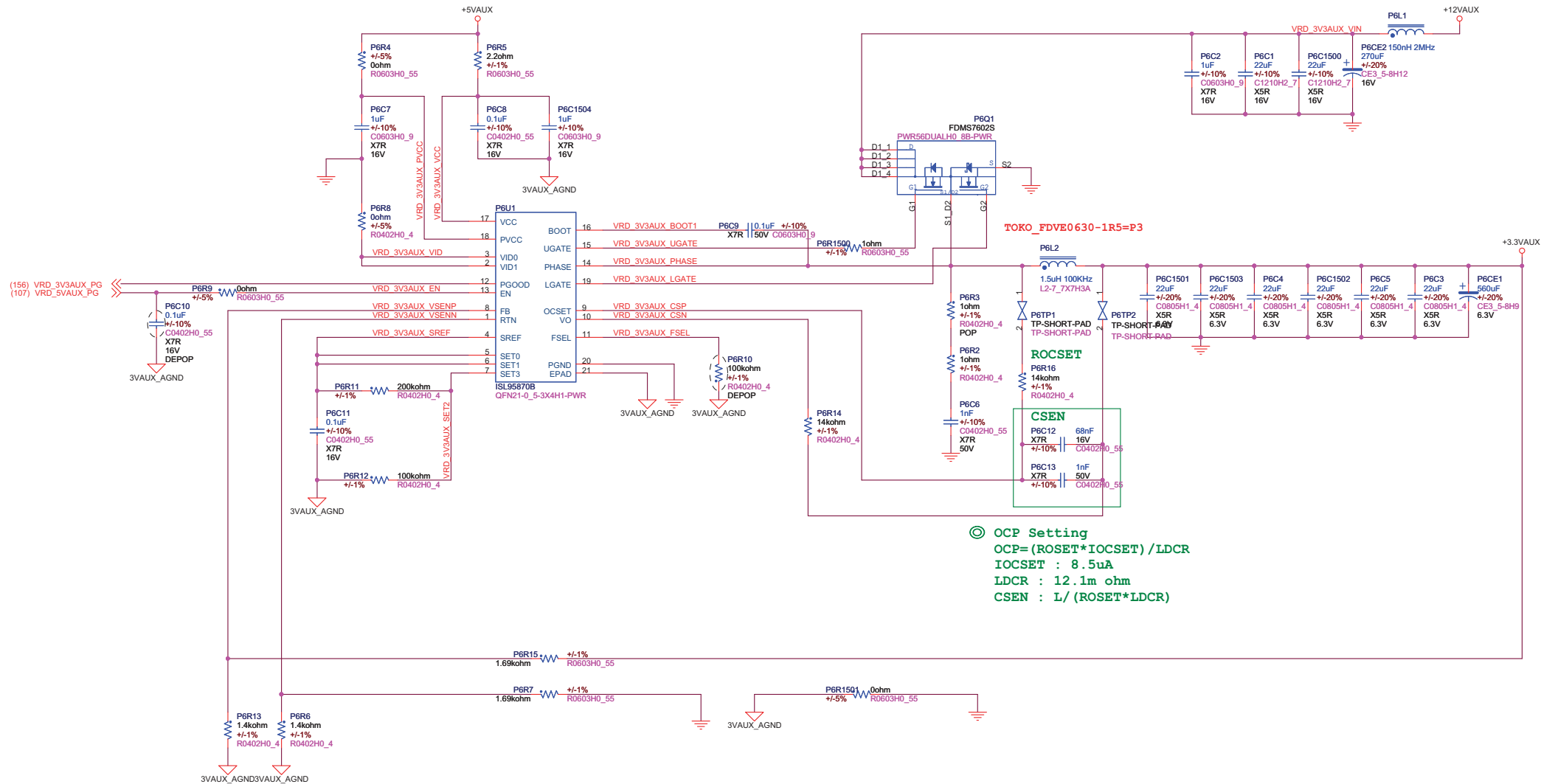
State	SINGLE_PS_PRES_N
0	Single PSU
1	Redundant PSU







+3.3VAUX



3V3AUX REGULATOR

VR:12VAUX->3.3VAUX

Controller:ISL95870B

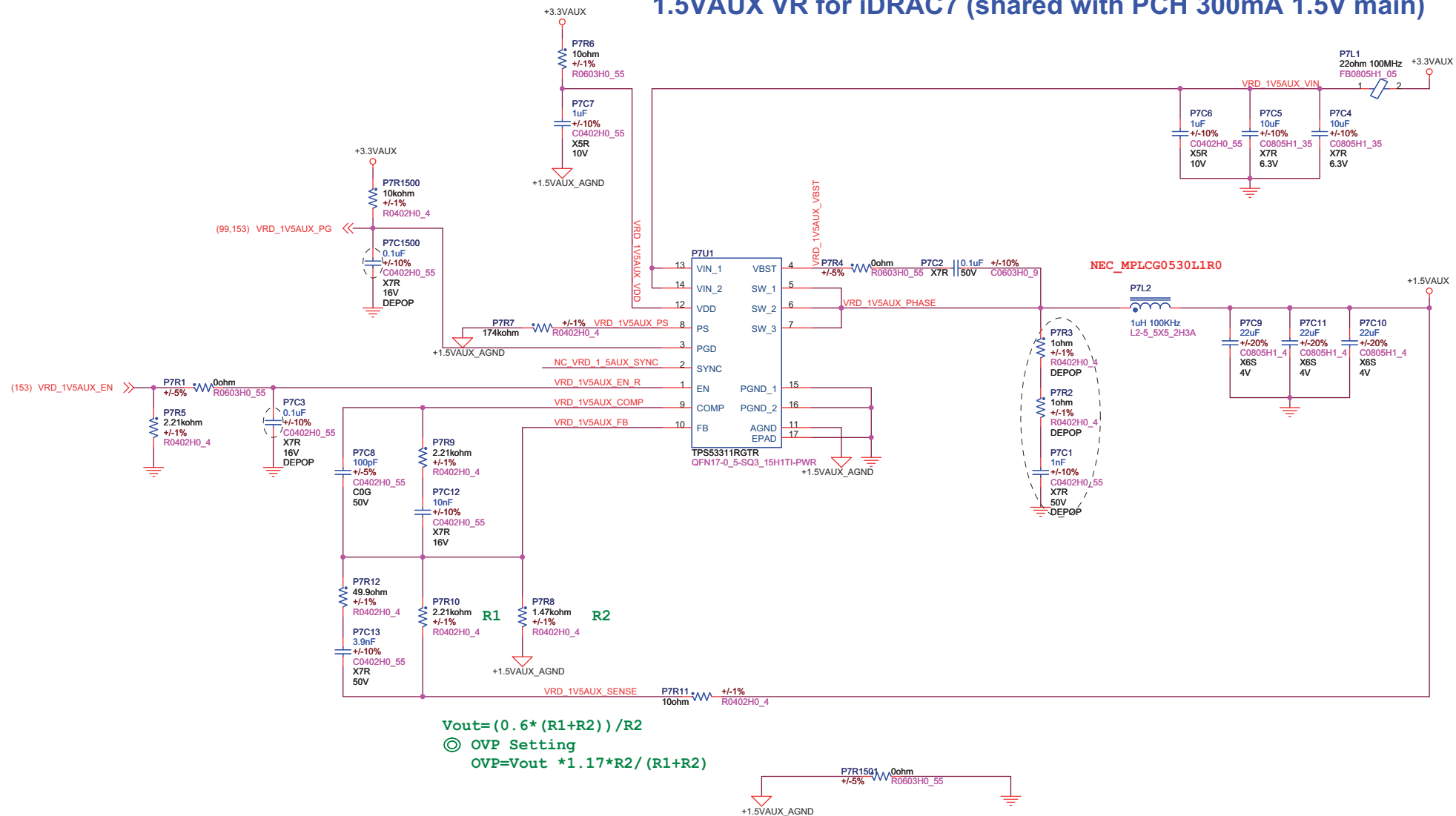
TDC=5.77A

Imax=7.21A

OCF=9.8A

Frequ=500KHz

1.5VAUX VR for iDRAC7 (shared with PCH 300mA 1.5V main)



1V5AUX REGULATOR

VR:3.3VAUX->1.5VAUX

Controller:TI53311

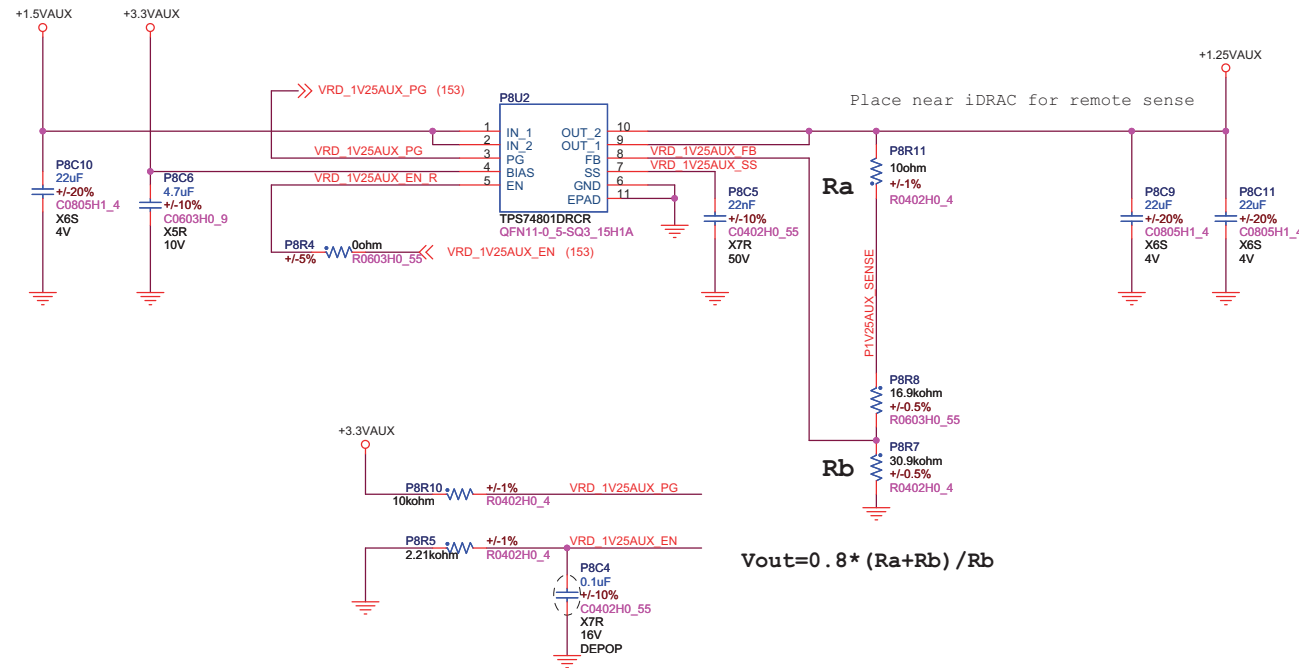
TDC=1.94A(include 1.5V main and downstream rails)

$$I_{\max} = 2.48 \text{ A}$$

OCP=4.5A(Fixed inside IC)

Frequ=1.1MHz

1.25VAUX Linear VR for iDRAC7



1V25AUX Linear VR

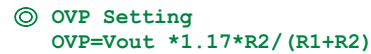
VR: 3.3VAUX->1.25VAUX


Controller: TPS74801

TDC=0.6A

Imax=0.75A

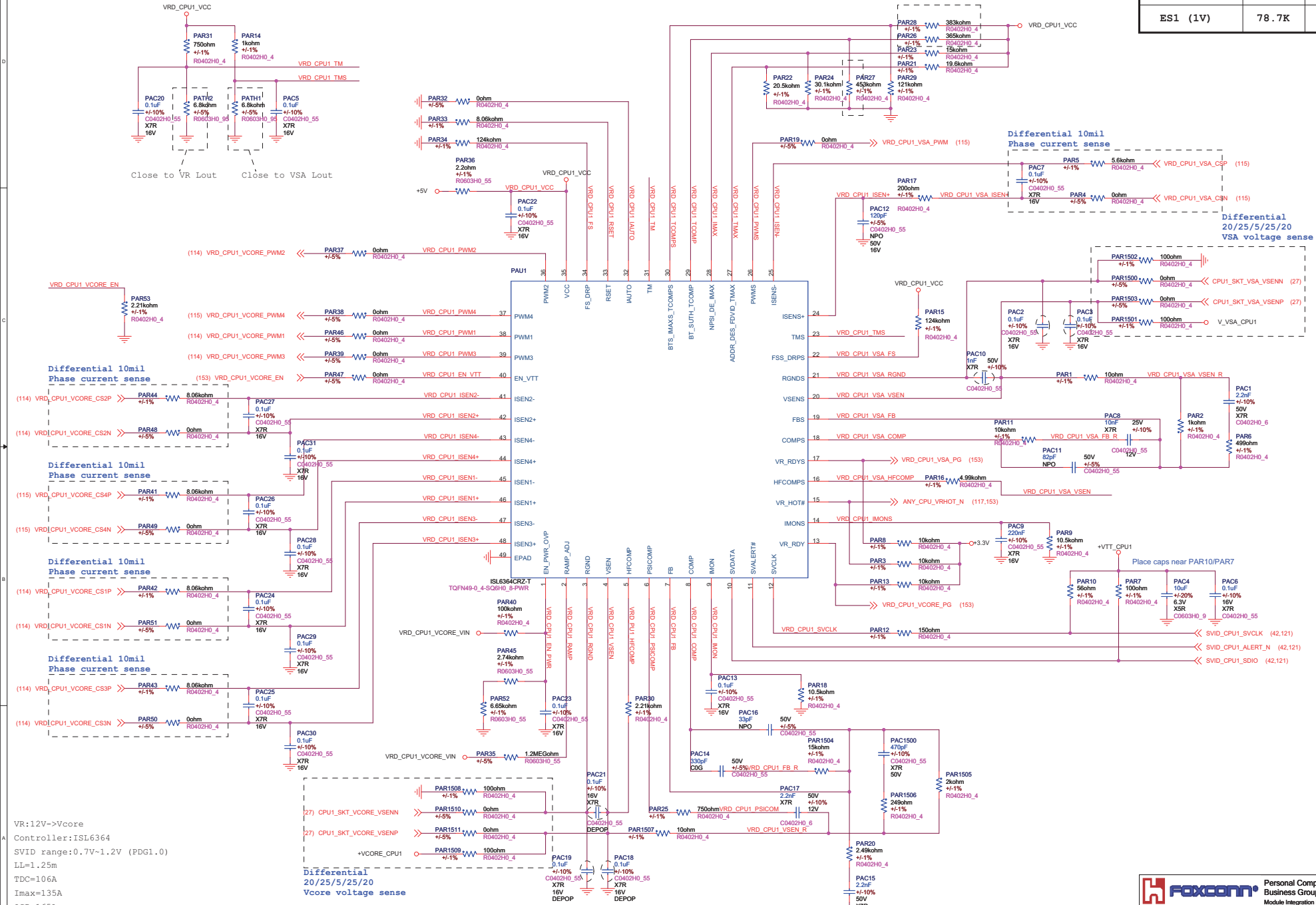
OCP=5.5A (Fixed inside IC)



 FOXCONN	Personal Computer & Enterprise Business Group (PCEBG)		
	Module Integration Business Group (MIBG)		
Hon Hai Precision Ind.Co., Ltd.			
Title			
VR:AUX Rails 1.1V			
Document Number:			
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12/25/2011 10:58 AM			

```
PAR28 will change 383K Ohm.
PAR26 will change 365K Ohm.
PAR27 will change 453K Ohm.
```

VBOOT setting	PAR26	PAR27
ES2 (0V)	365K	453K
ES1 (1V)	78.7K	97.6K



FOXCONN Personal Computer & Enterprise
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Title	CPU1 VCORE & VSA
-------	------------------

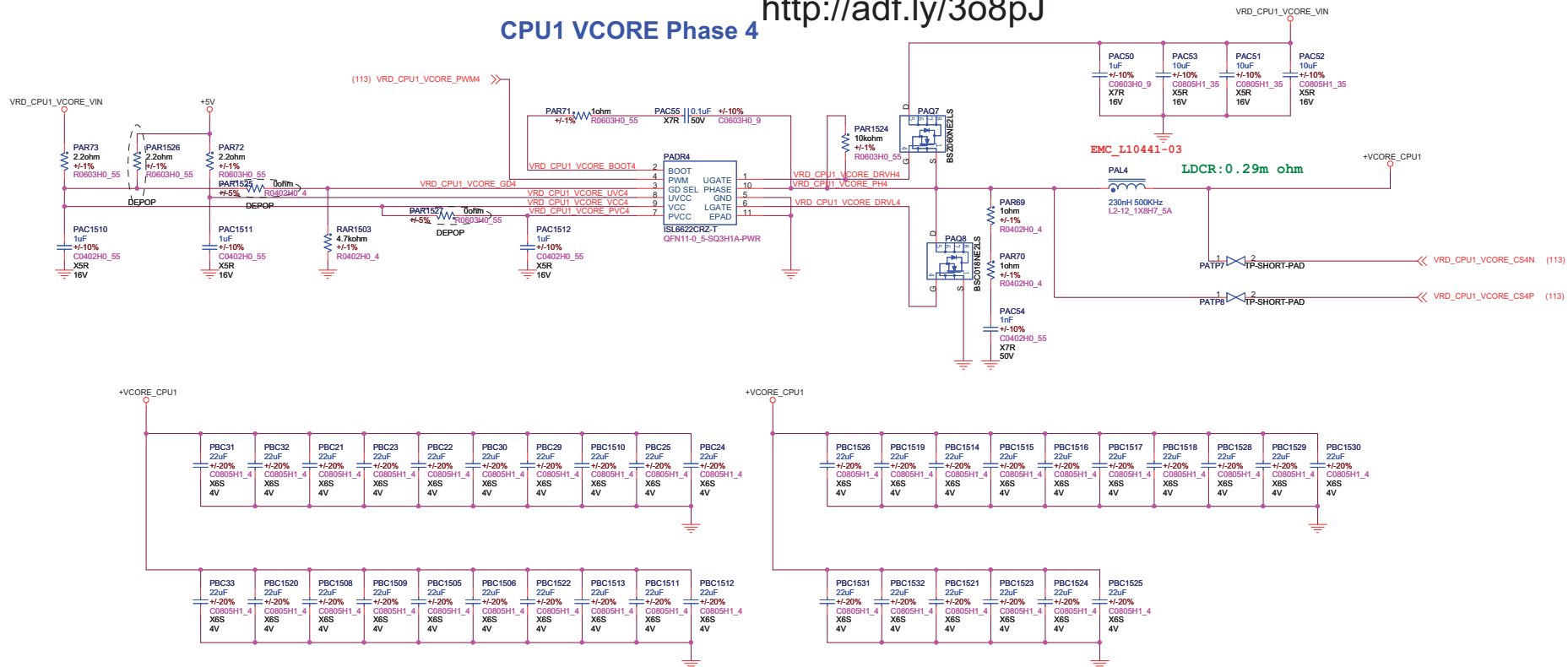
Document Number:
PCB P/N: 01015C800-000-G

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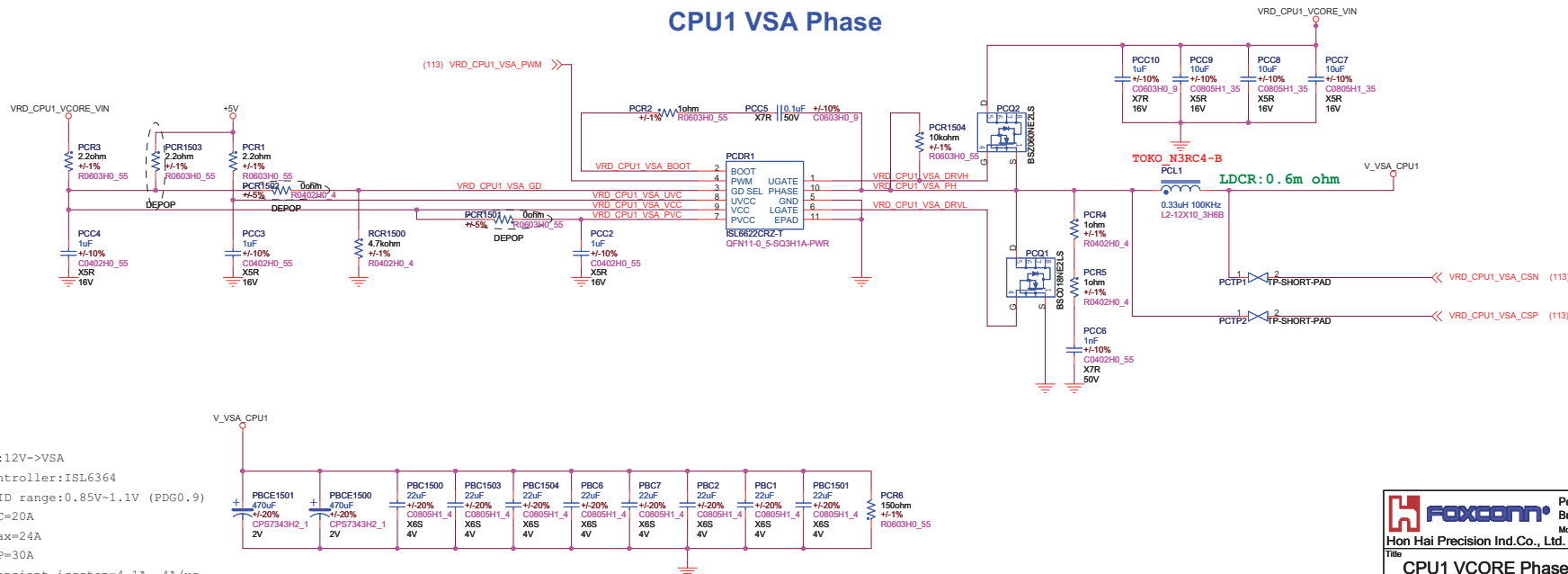
<http://adf.ly/3o8pJ>



CPU1 VCORE Phase 4



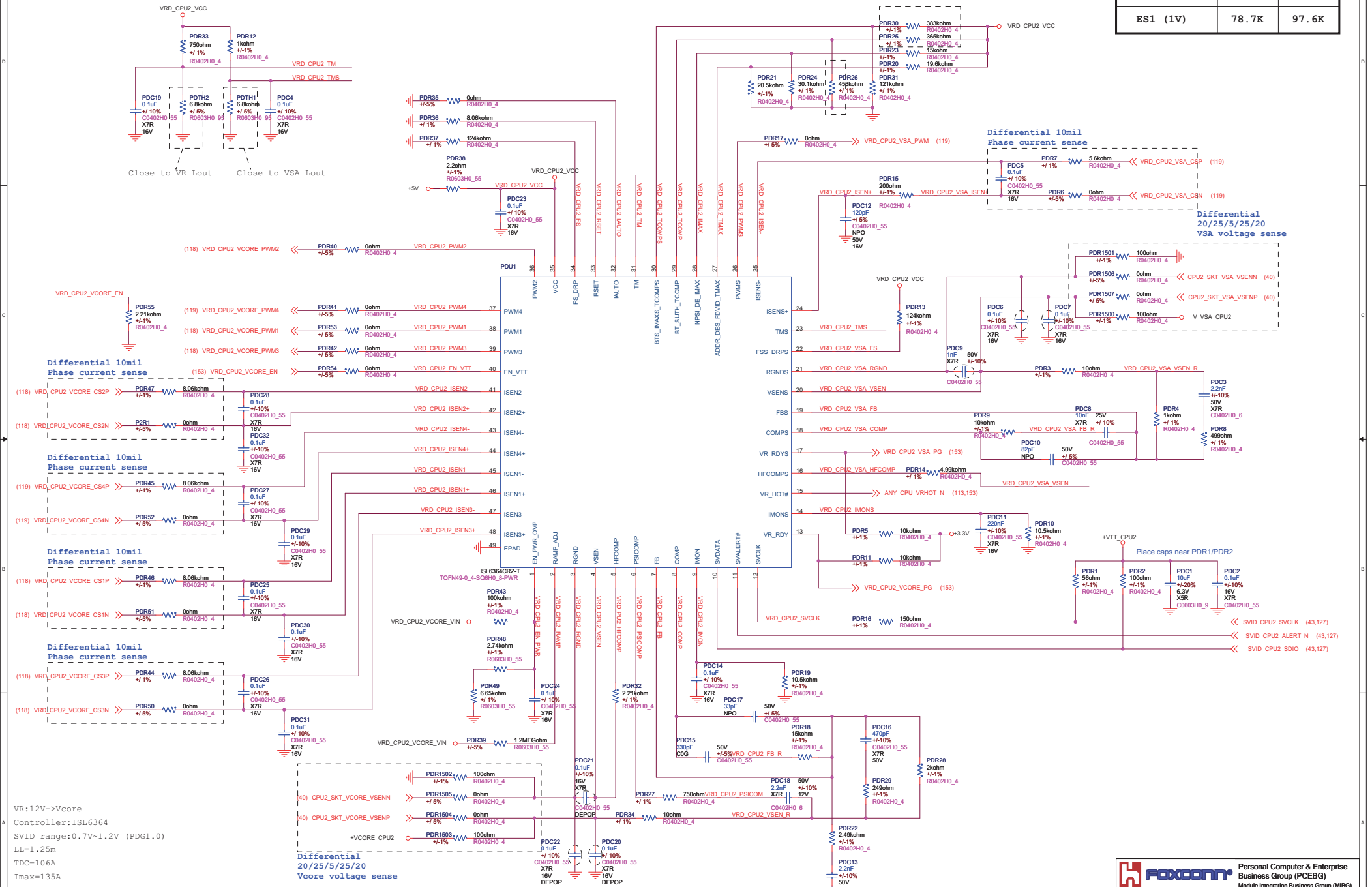
CPU1 VSA Phase



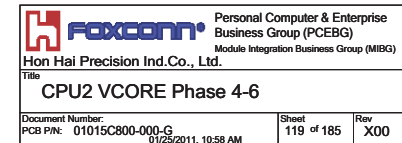
VR:12V->VSA
Controller:ISL6364
SVID range:0.85V~1.1V (PDG0.9)
TDC=20A
Imax=24A
OCP=30A
Transient iccstep=4.1A, 4A/us
Frequ=403KHz

PDR30 will change 383K Ohm.
PDR25 will change 365K Ohm.
PDR26 will change 453K Ohm.

VBOOT setting	PDR25	PDR26
ES2 (0V)	365K	453K
ES1 (1V)	78.7K	97.6K



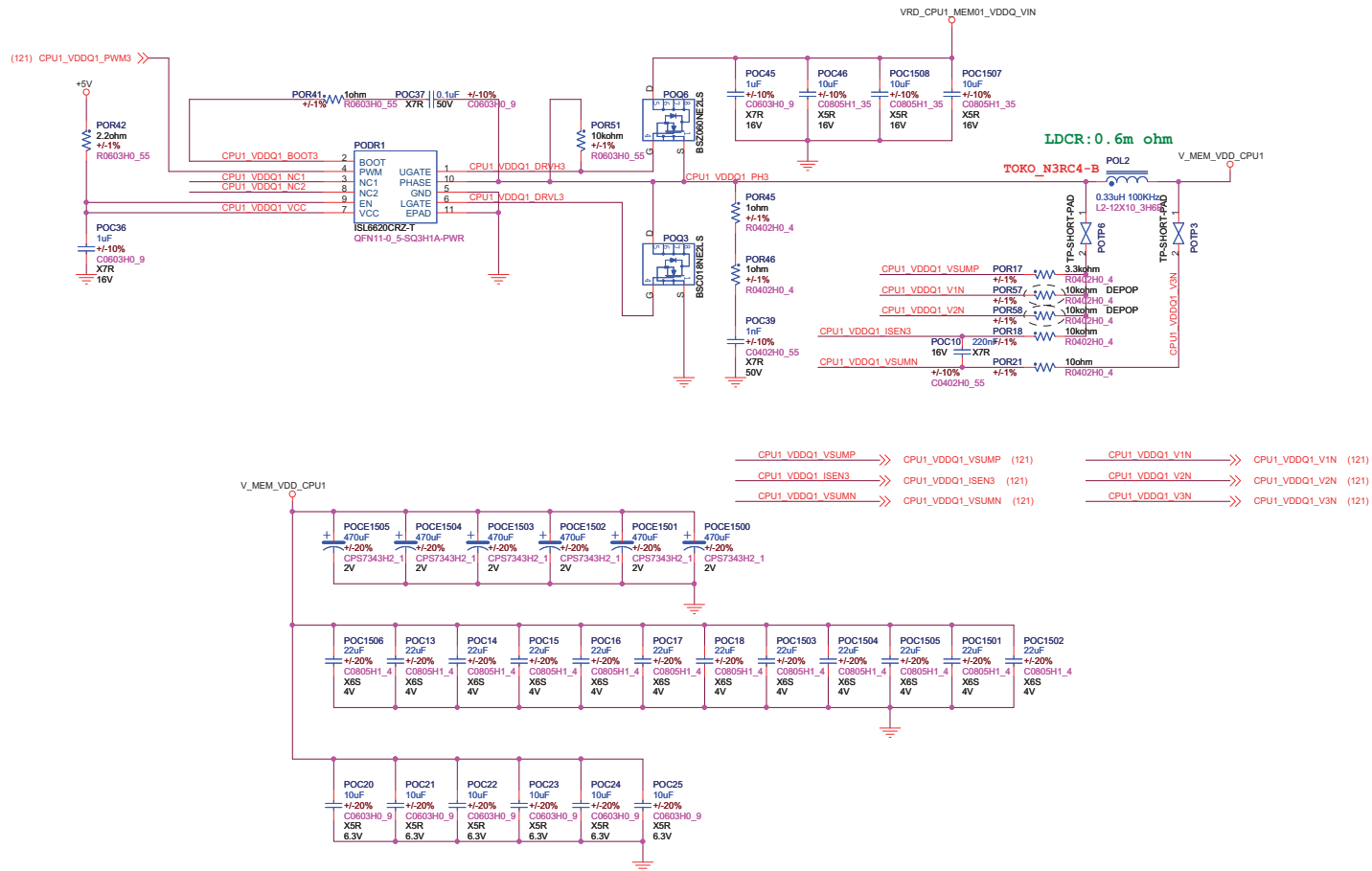
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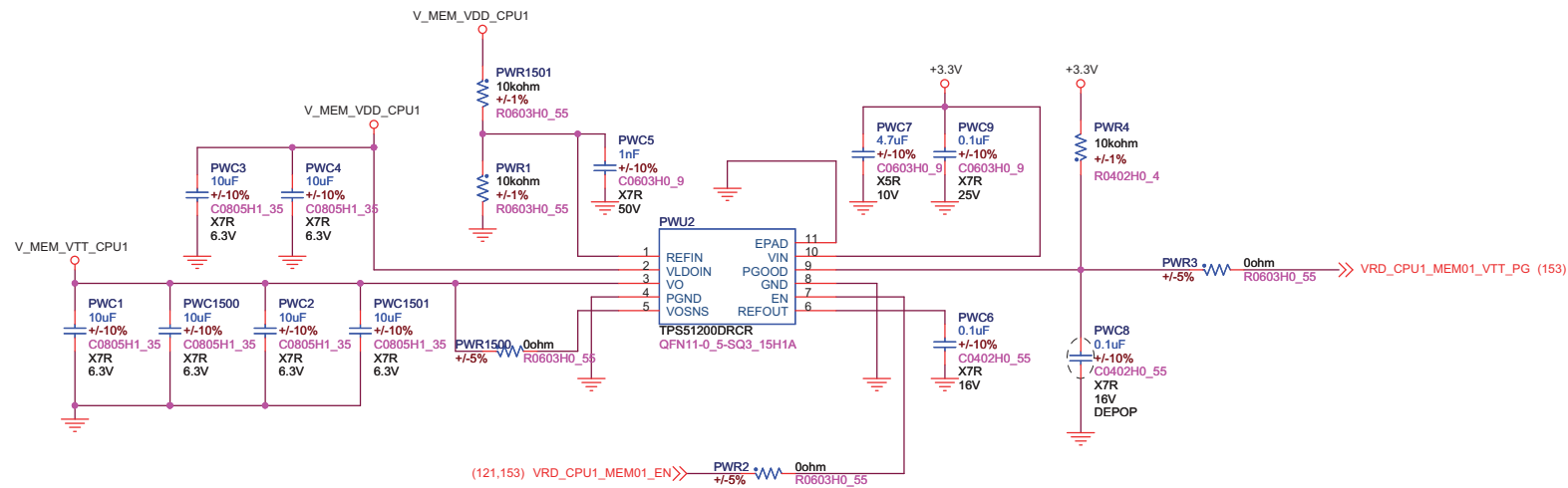
<http://adf.ly/3o8pJ>



CPU1 MEM1 VDDQ

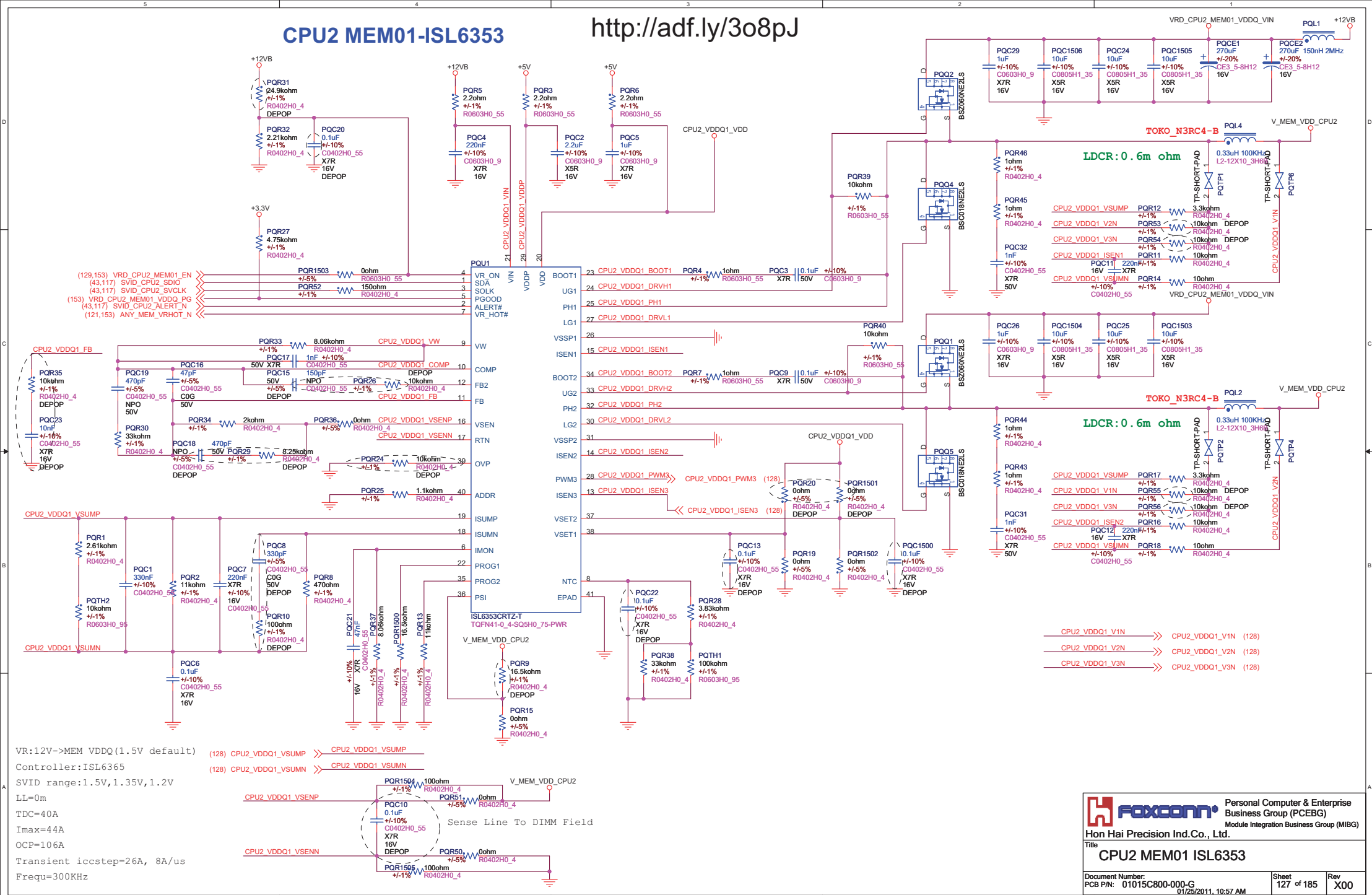


CPU1 MEM01 VTT

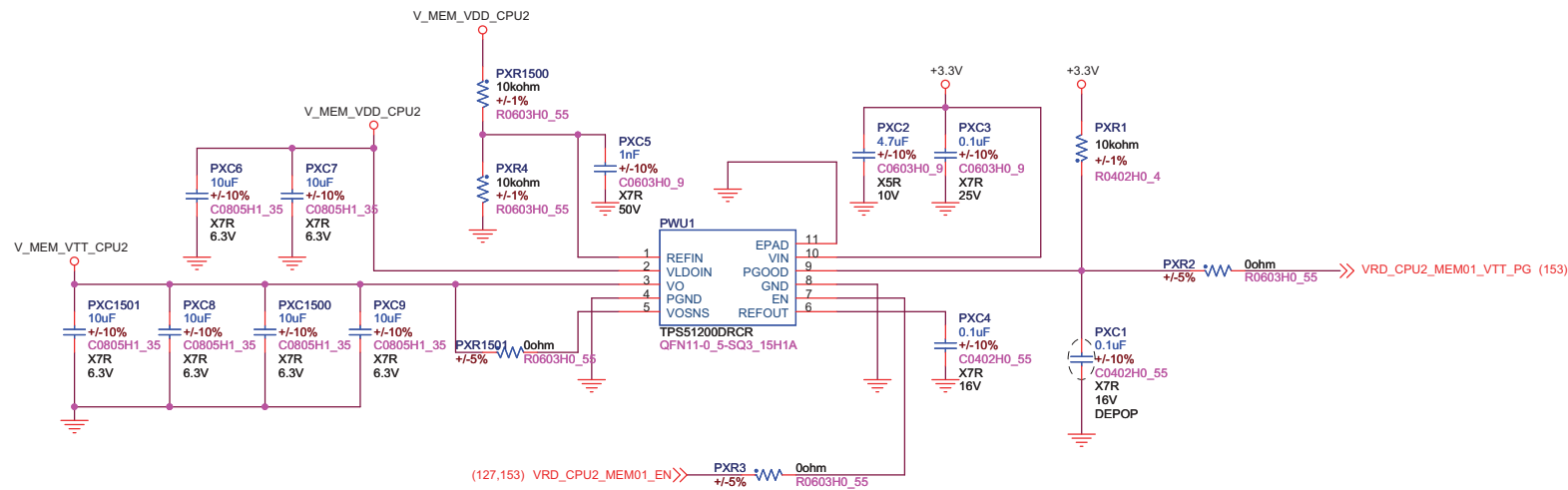


VR:MEM VDD->MEM VTT(1/2 VDDQ)
 Controller:TPS51200
 TDC=3.9A
 Imax=4.3A
 OCP=3A
 Transient iccstep=0.4A, 1A/us

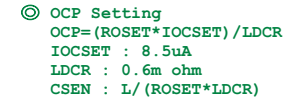
CPU2 MEM01-ISL6353


<http://adf.ly/3o8pJ>

CPU2 MEM01 VTT

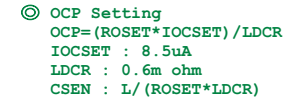



VR:12V->MEM VTT (1/2 VDDQ)
 Controller:TPS51200
 TDC=3.9A
 I_{max}=4.3A
 OCP=3A
 Transient iccstep=0.4A, 1A/us



 FOXCONN®	Personal Computer & Enterprise Business Group (PCEBG)		
	Module Integration Business Group (MIBG)		
Hon Hai Precision Ind. Co., Ltd.			
Title			
CPU1 VTT			
Document Number: PCB P/N: 0101SC800-000-G 01/25/2011, 10:58 AM		Sheet 133 of 185	Rev X00

CPU2 VTT



 FOXCONN	Personal Computer & Enterprise Business Group (PCEBG)		
	Module Integration Business Group (MIBG)		
Hon Hai Precision Ind. Co., Ltd.			
Title			
CPU2 VTT			
Document Number: PCB P/N: 0101SC800-000-G 01/25/2011, 10:58 AM		Sheet 134 of 185	Rev X00

<http://adf.ly/3o8pJ>

CPU1 PLL

PMU1/PMU51 is configured to DE Master/Slave pair

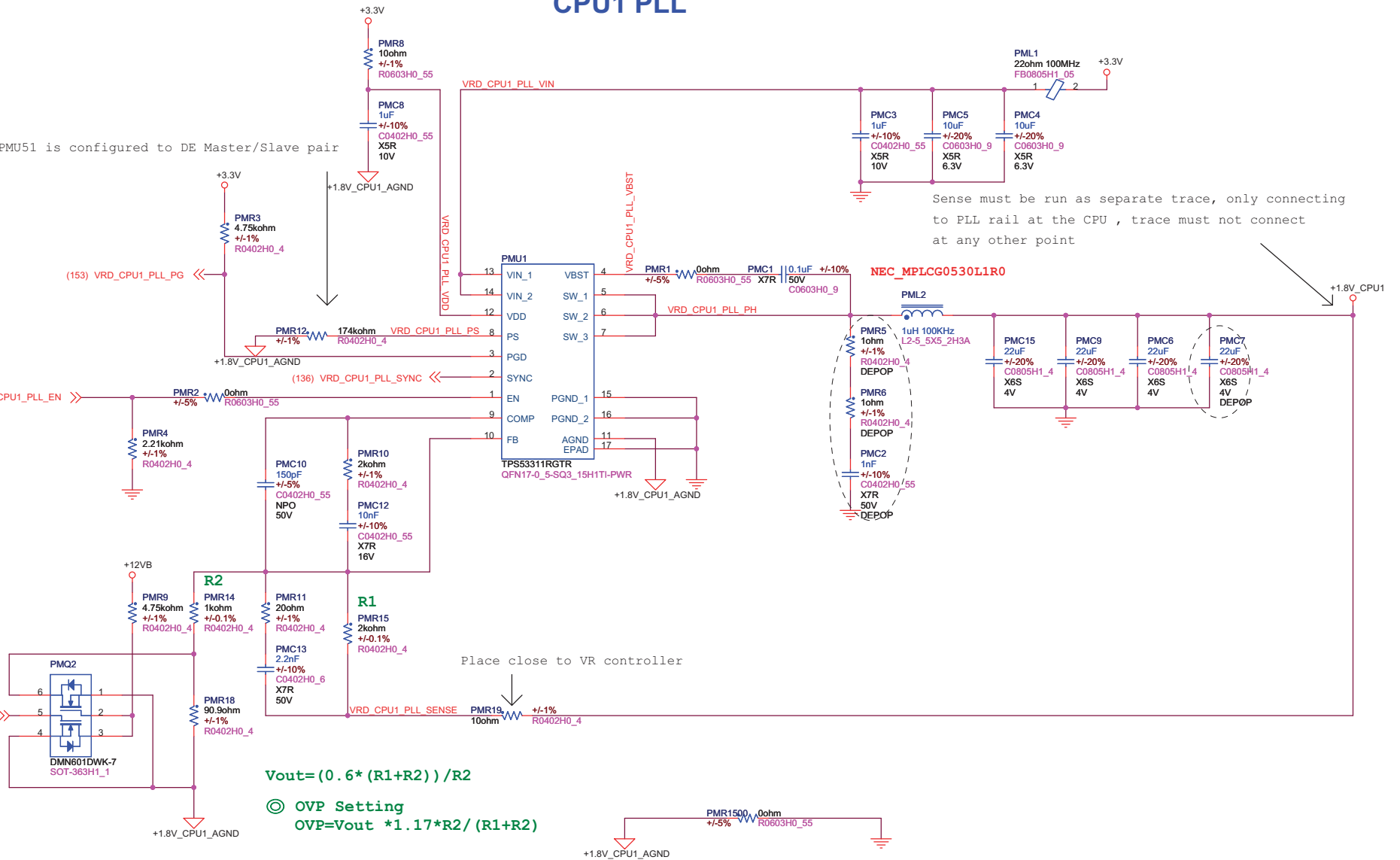
Sense must be run as separate trace, only connecting to PLL rail at the CPU, trace must not connect at any other point

H:1.7V-Ivy Bridge
L:1.8V-Sandy Bridge

$$V_{out} = (0.6 * (R1 + R2)) / R2$$

© OVP Setting
 $OVP = V_{out} * 1.17 * R2 / (R1 + R2)$

3.3V->1.8/1.7V
Controller:TPS53311
TDC=1.5A
Imax=2A
OCP=4.5A Fixed inside IC
Frequ=1MHz



http://adf.ly/3o8pJ

CPU2 PLL

PMU1/PMU51 is configured to DE Master/Slave pair

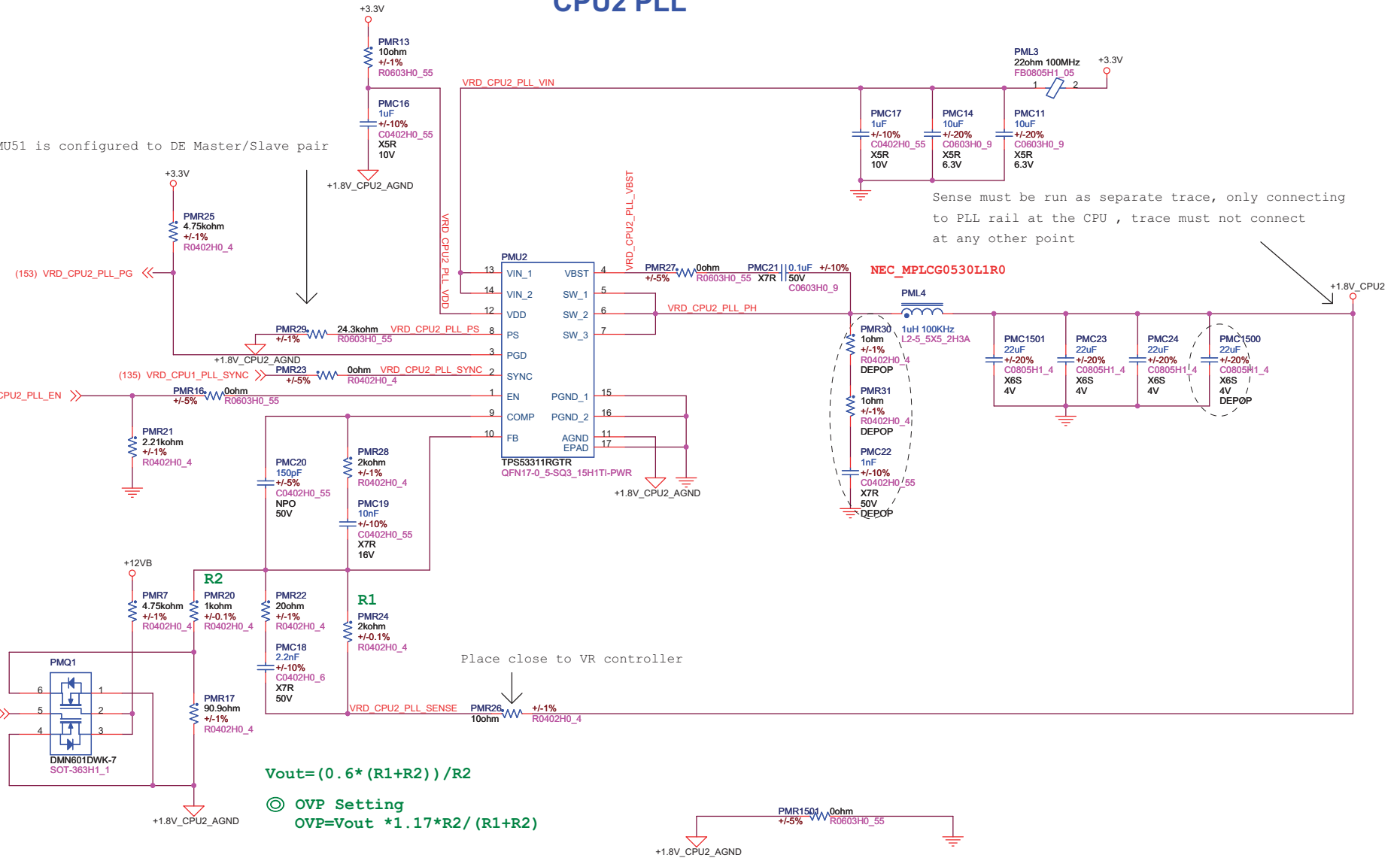
Sense must be run as separate trace, only connecting to PLL rail at the CPU, trace must not connect at any other point

H:1.7V-Ivy Bridge
L:1.8V-Sandy Bridge

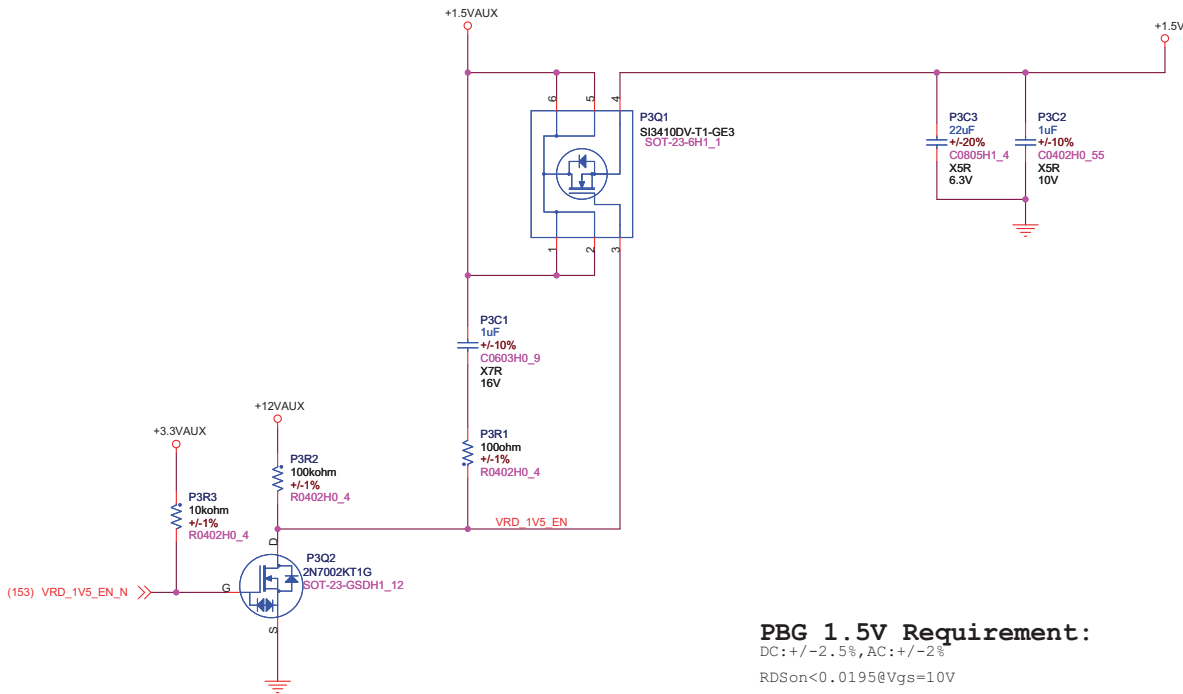
$$V_{out} = (0.6 * (R1 + R2)) / R2$$

⊙ OVP Setting
OVP = $V_{out} * 1.17 * R2 / (R1 + R2)$

3.3V->1.8/1.7V
Controller:TPS53311
TDC=1.5A
Imax=2A
OCP=4.5A Fixed inside IC
Frequ=1MHz



PBG 1.5V

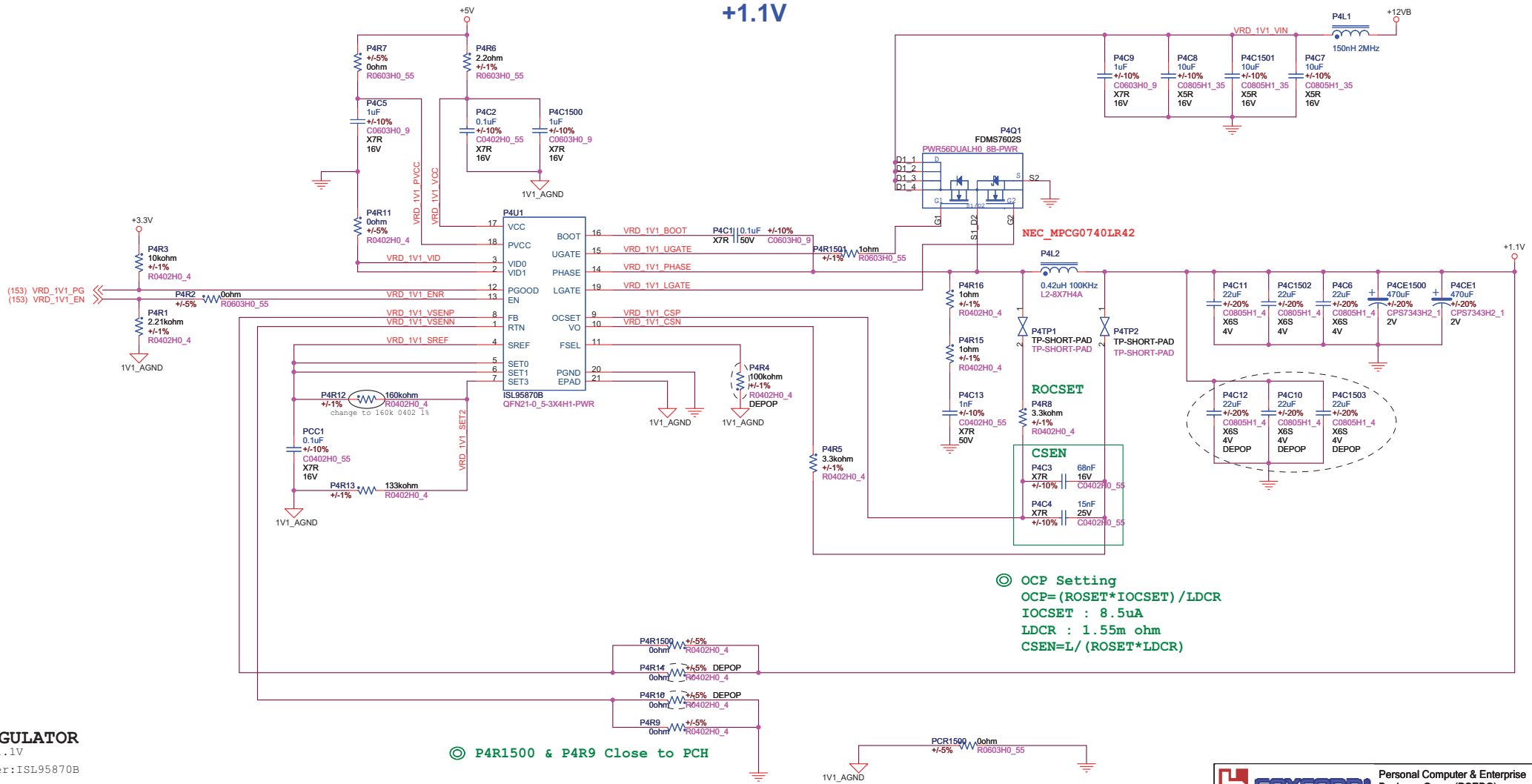


PBG 1.5V Requirement:

DC: +/-2.5%, AC: +/-2%
RDSon<0.0195@Vgs=10V
Vdroup=0.5A*0.0195=0.00975V=>6.5%
Ploss=0.5A*0.5A*0.0195=4.8mW

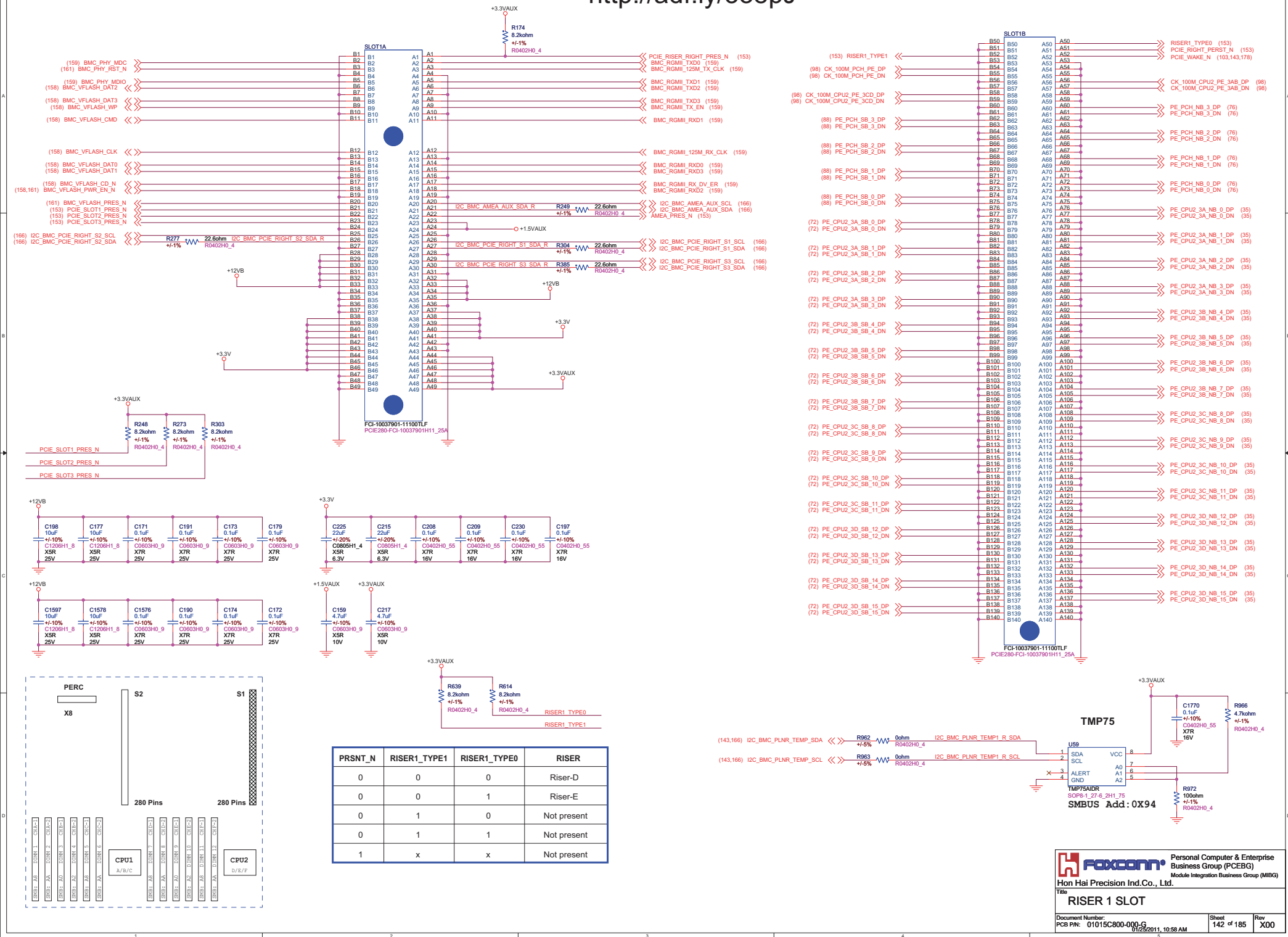
1V5 Load Switch

VR:1.5VAUX->1.5V
TDC=0.4A
Imax=0.5A
OCP=NA



Note: Base on Intel suggestion, PCIe connector routing requirement on romley platform at PCIe3 speed that NC pin should be terminated on-n-blair.

<http://adf.ly/3o8pJ>



http://adf.ly/3o8pJ



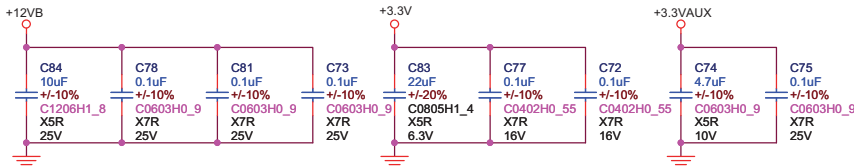
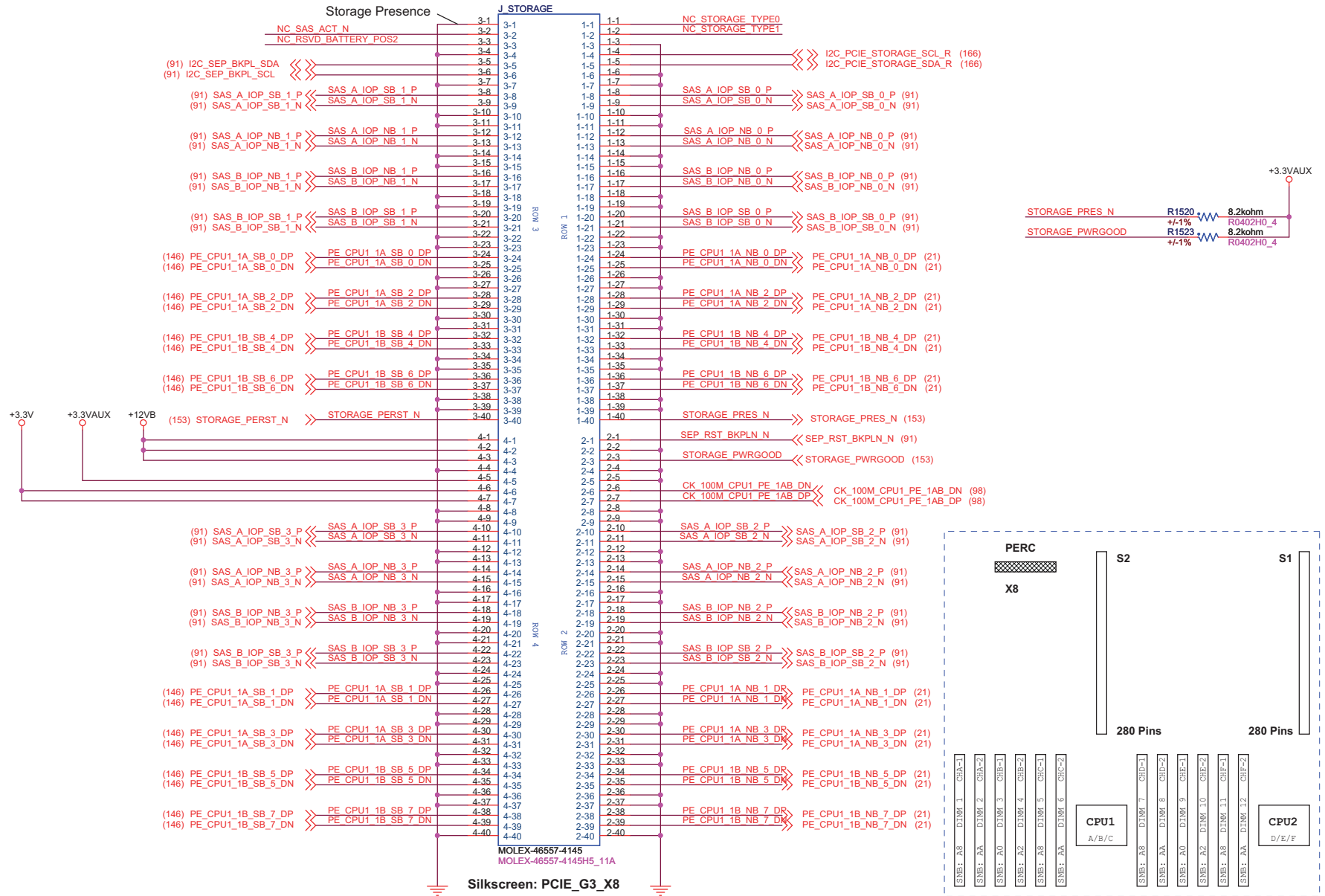
PRSN_T_N	RISR2_TYPE1	RISR2_TYPE0	RISER
0	0	0	Riser-A
0	0	1	Riser-B
0	1	0	Riser-C
0	1	1	Riser-F
1	x	x	Not present

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Module Integration Business Group (MIBG)

Hon Hai Precision Ind.Co., Ltd.	
Title	RISER 2 SLOT

(21) PE_CPU1_1B_SB_7_C_DP	C56	220nF +/-10% 16V X7R	PE_CPU1_1B_SB_7_DP (147)
(21) PE_CPU1_1B_SB_6_C_DP	C58	220nF +/-10% 16V X7R	PE_CPU1_1B_SB_6_DP (147)
(21) PE_CPU1_1B_SB_5_C_DP	C60	220nF +/-10% 16V X7R	PE_CPU1_1B_SB_5_DP (147)
(21) PE_CPU1_1B_SB_4_C_DP	C62	220nF +/-10% 16V X7R	PE_CPU1_1B_SB_4_DP (147)
(21) PE_CPU1_1B_SB_7_C_DN	C57	220nF +/-10% 16V X7R	PE_CPU1_1B_SB_7_DN (147)
(21) PE_CPU1_1B_SB_6_C_DN	C59	220nF +/-10% 16V X7R	PE_CPU1_1B_SB_6_DN (147)
(21) PE_CPU1_1B_SB_5_C_DN	C61	220nF +/-10% 16V X7R	PE_CPU1_1B_SB_5_DN (147)
(21) PE_CPU1_1B_SB_4_C_DN	C63	220nF +/-10% 16V X7R	PE_CPU1_1B_SB_4_DN (147)
(21) PE_CPU1_1A_SB_3_C_DP	C64	220nF +/-10% 16V X7R	PE_CPU1_1A_SB_3_DP (147)
(21) PE_CPU1_1A_SB_2_C_DP	C66	220nF +/-10% 16V X7R	PE_CPU1_1A_SB_2_DP (147)
(21) PE_CPU1_1A_SB_1_C_DP	C68	220nF +/-10% 16V X7R	PE_CPU1_1A_SB_1_DP (147)
(21) PE_CPU1_1A_SB_0_C_DP	C70	220nF +/-10% 16V X7R	PE_CPU1_1A_SB_0_DP (147)
(21) PE_CPU1_1A_SB_3_C_DN	C65	220nF +/-10% 16V X7R	PE_CPU1_1A_SB_3_DN (147)
(21) PE_CPU1_1A_SB_2_C_DN	C67	220nF +/-10% 16V X7R	PE_CPU1_1A_SB_2_DN (147)
(21) PE_CPU1_1A_SB_1_C_DN	C69	220nF +/-10% 16V X7R	PE_CPU1_1A_SB_1_DN (147)
(21) PE_CPU1_1A_SB_0_C_DN	C71	220nF +/-10% 16V X7R	PE_CPU1_1A_SB_0_DN (147)

MONOLITHIC



FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)

Hon Hai Precision Ind. Co., Ltd.

Title: **STORAGE**

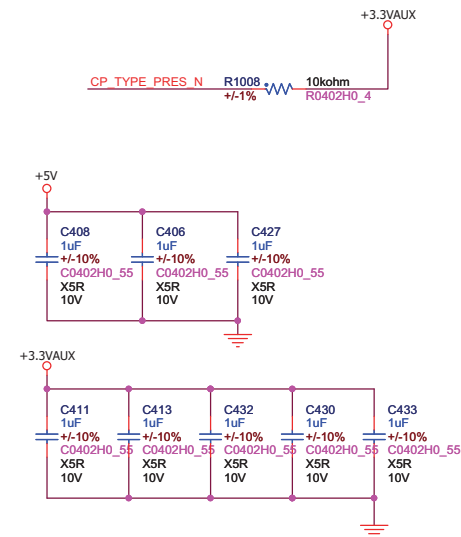
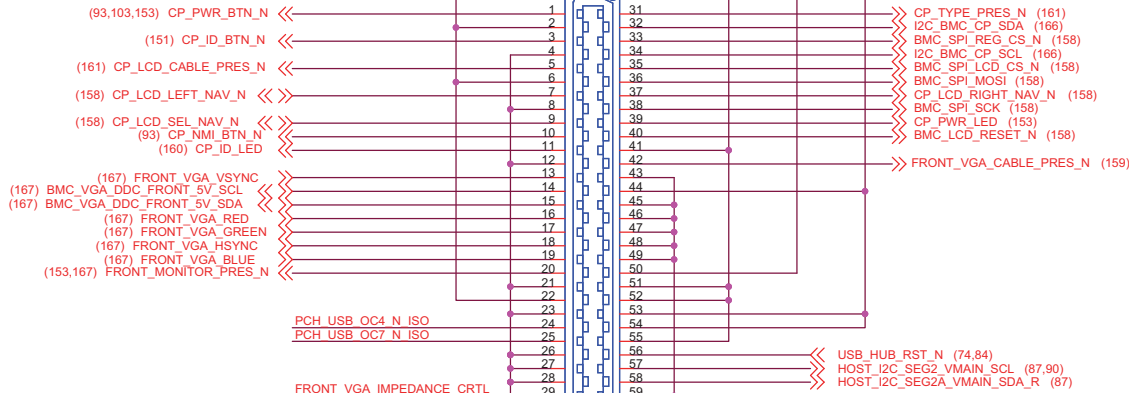
Document Number: 01015C800-000-G
PCB P/N: 01015C800-000-G

01/25/2011, 10:57 AM

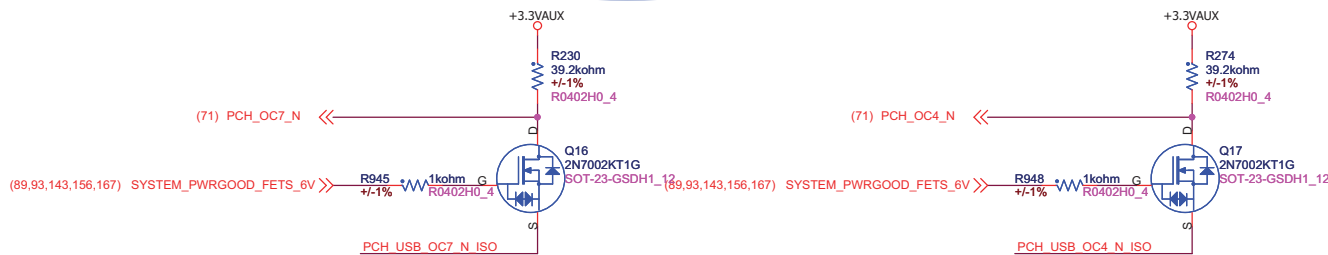
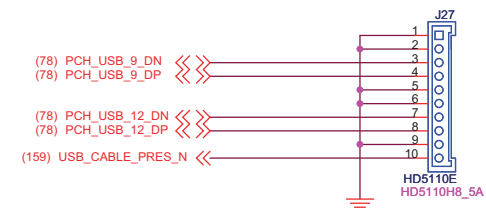
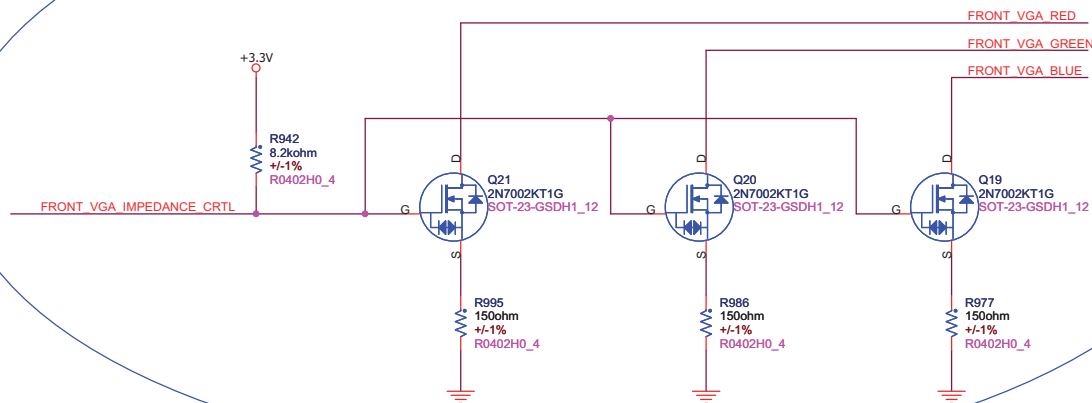
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Rev X00

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State	FRONT_VGA_IMPEDANCE_CRTL
0	50 Ohm
1	75 Ohm



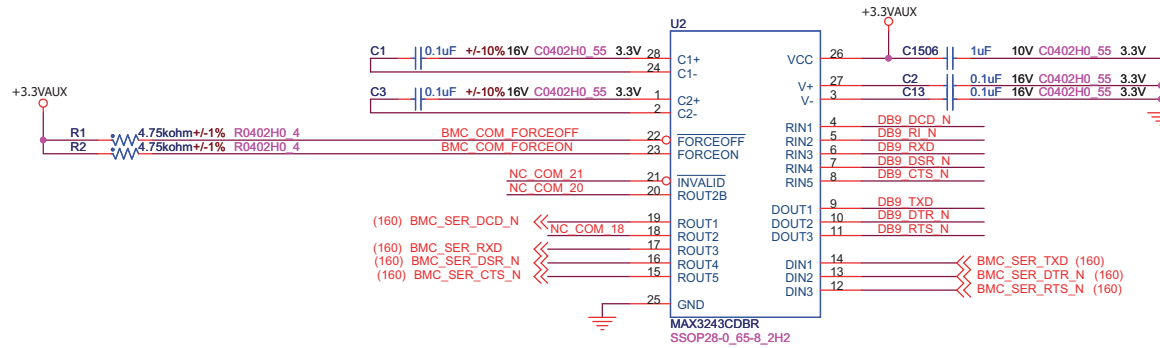
FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)
Hon Hai Precision Ind. Co., Ltd.

Control Panel

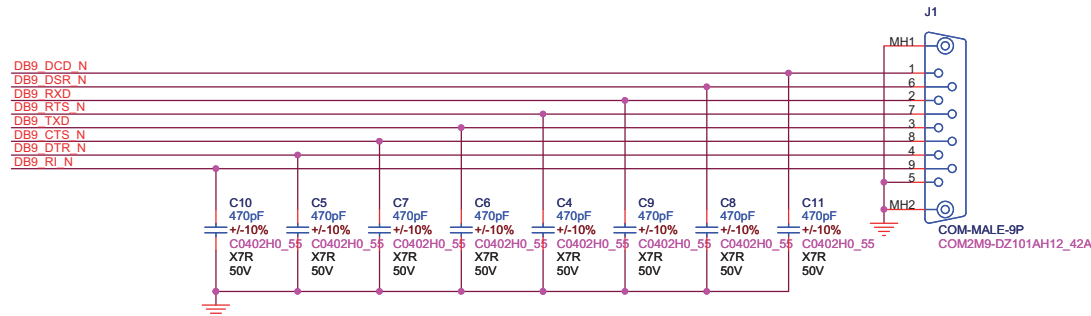
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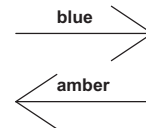
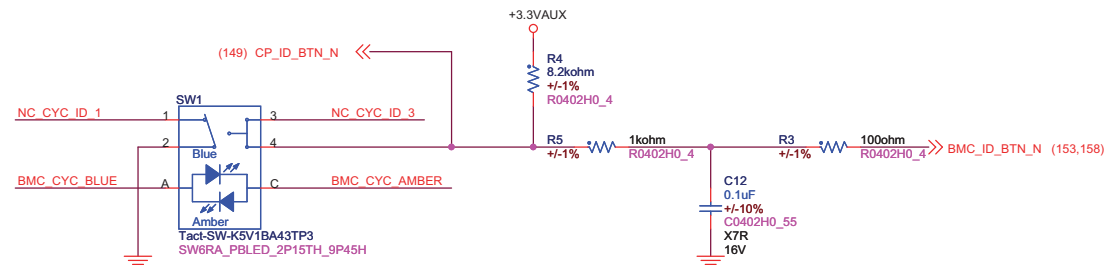
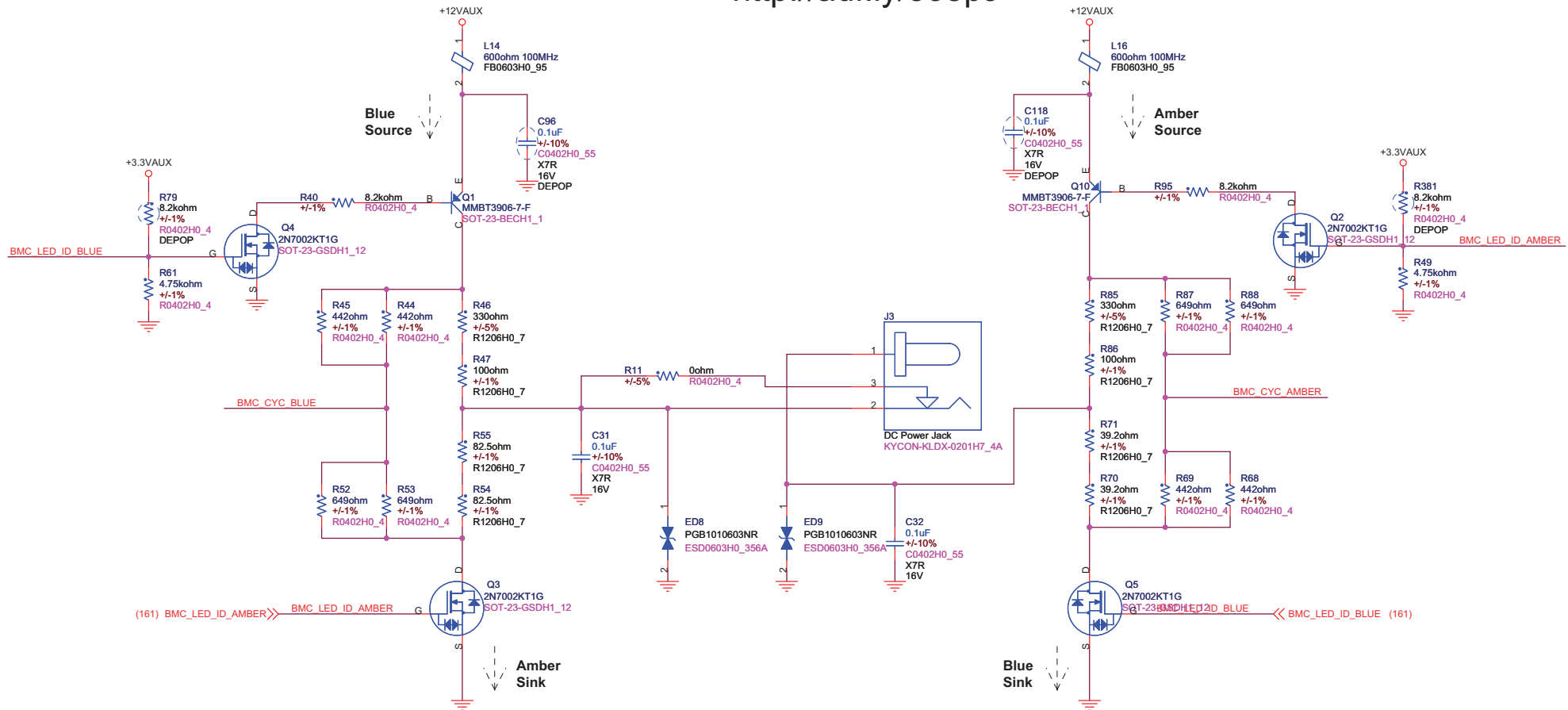
Sheet 149 of 185
Rev X00

SYSTEM SERIAL

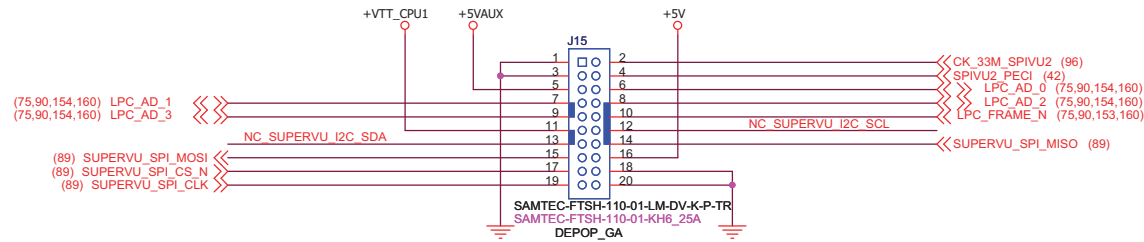


COM Port

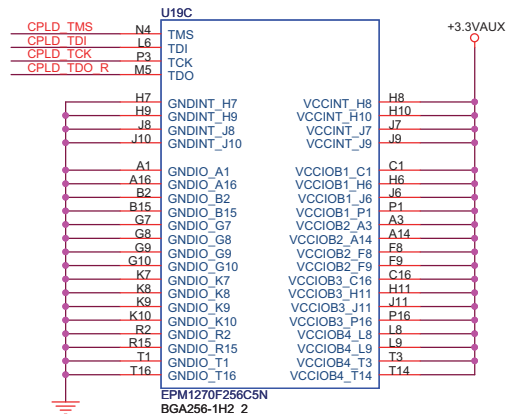




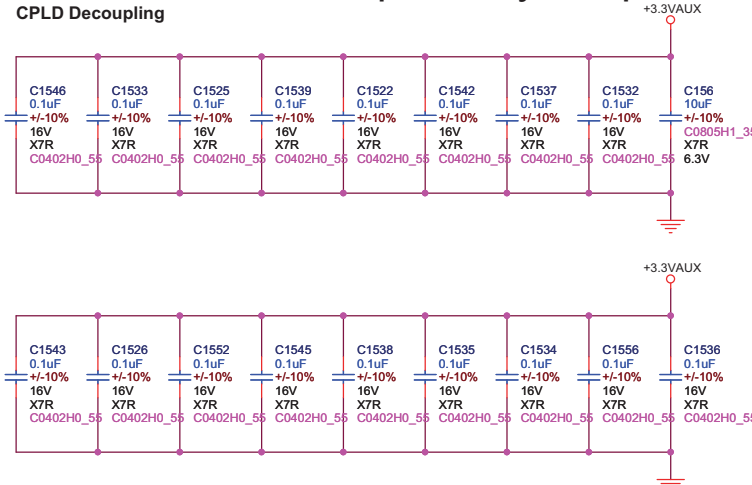
SVU-2 Connector



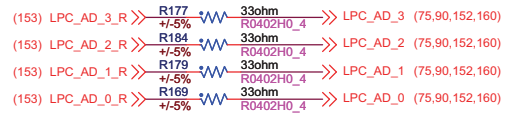




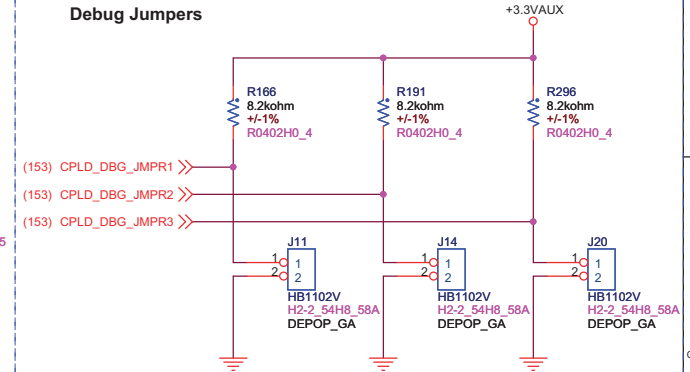
CPLD Decoupling



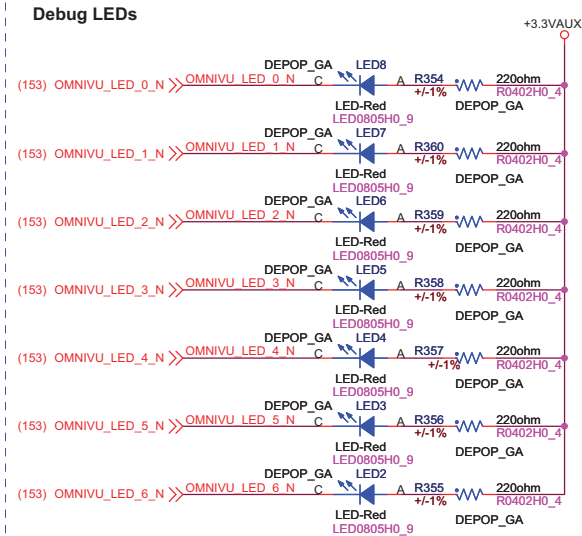
Series Rs



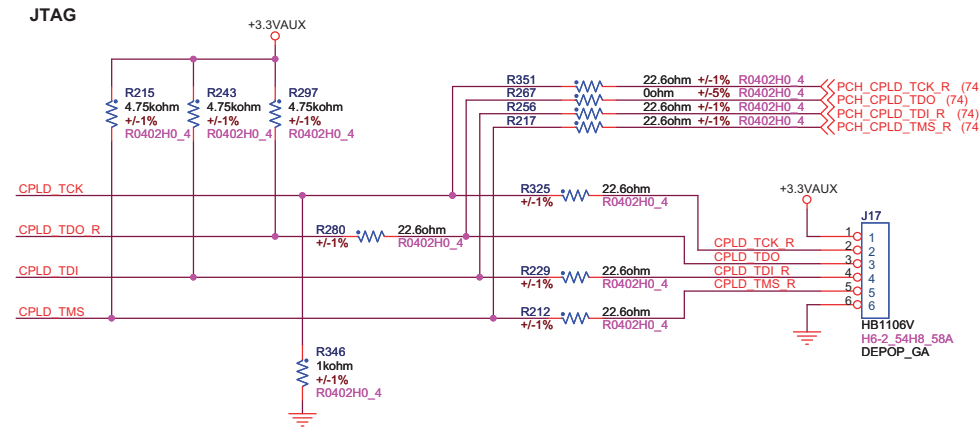
Debug Jumpers



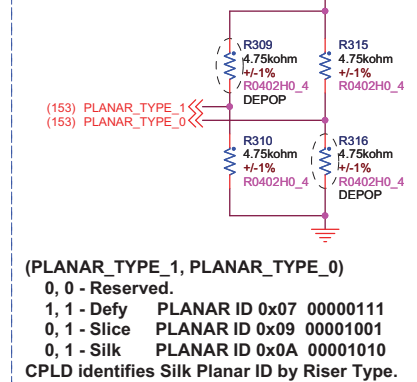
Debug LEDs



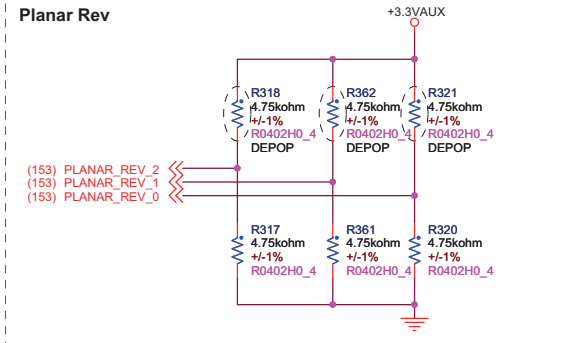
JTAG



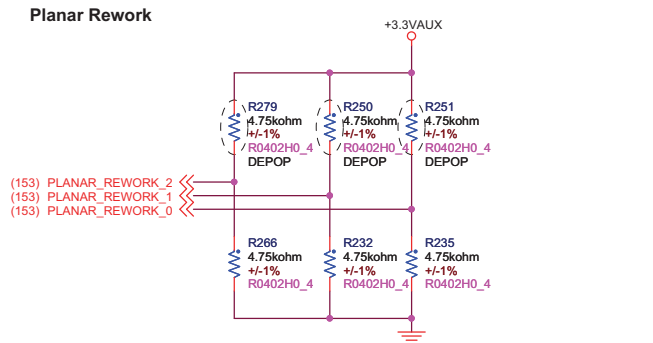
Planar Type



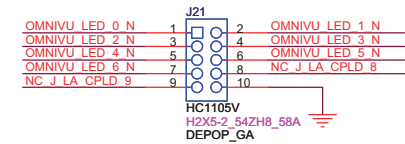
Planar Rev



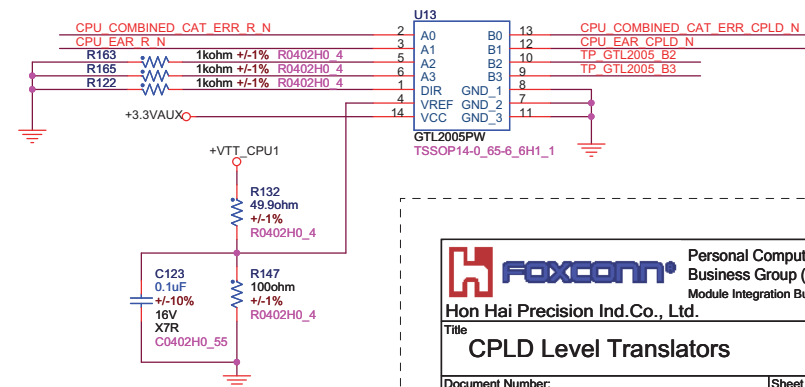
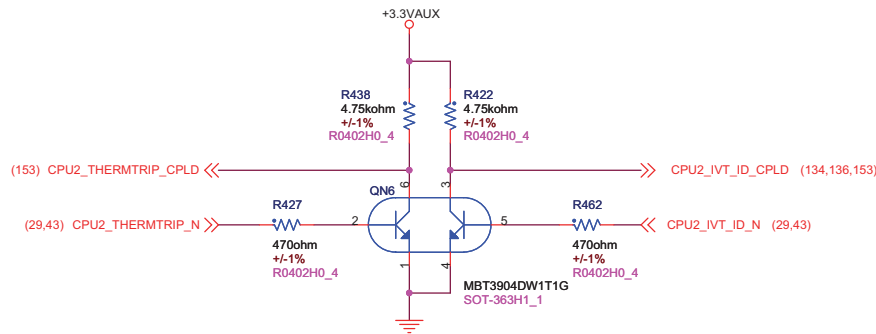
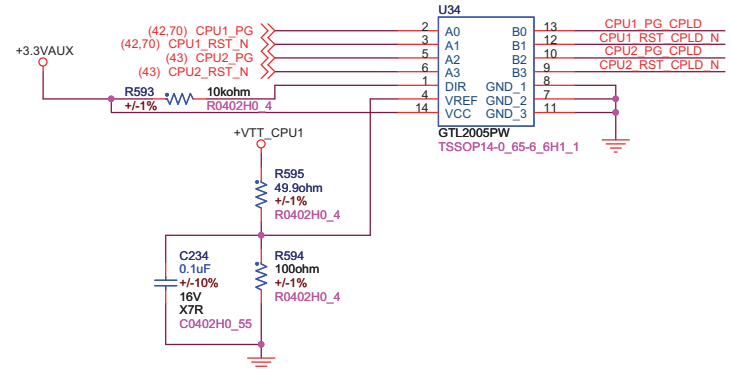
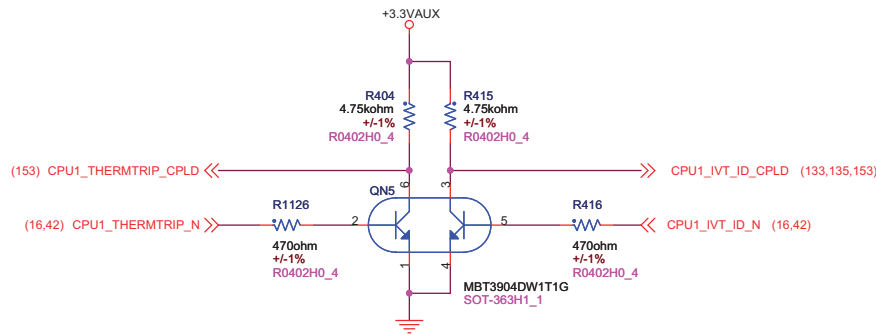
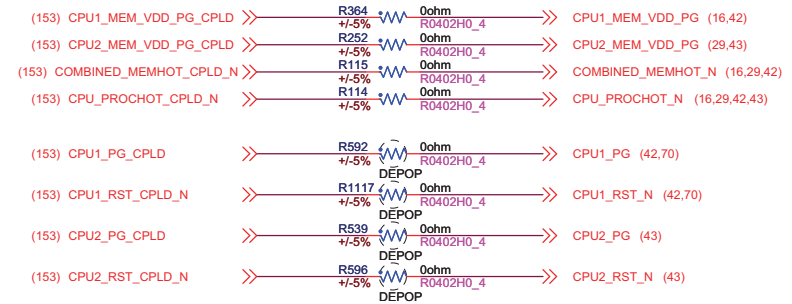
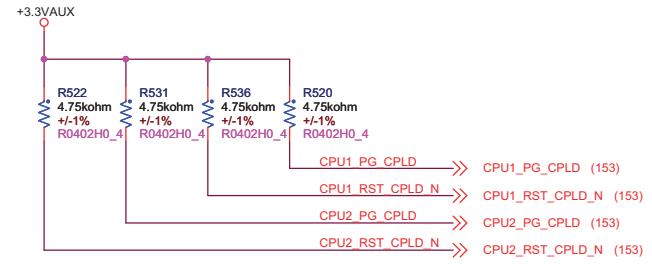
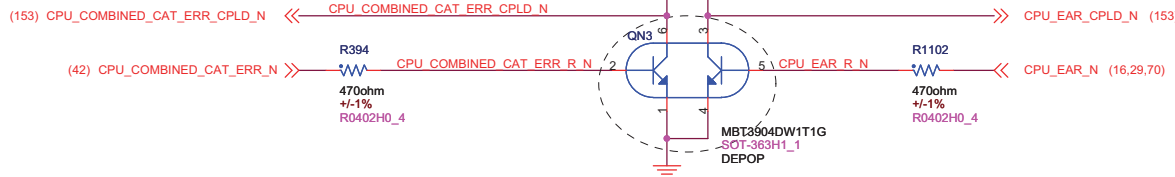
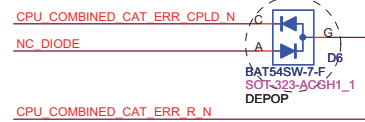
Planar Rework



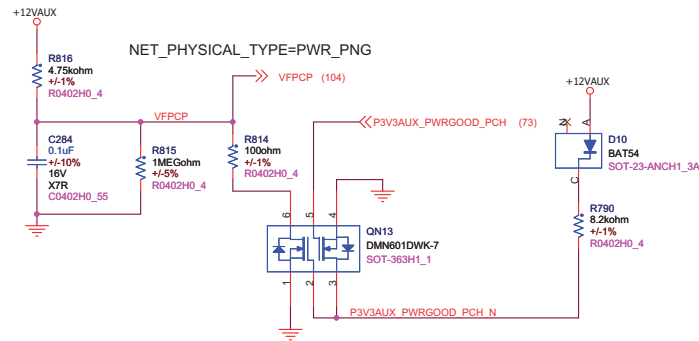
Logic Analyzer Debug Connector



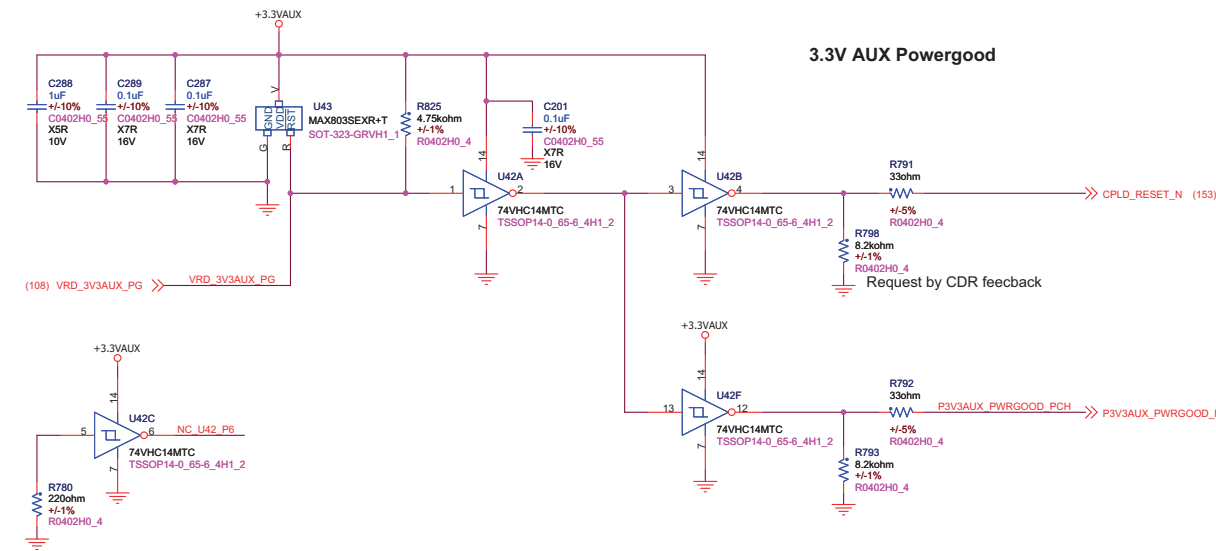
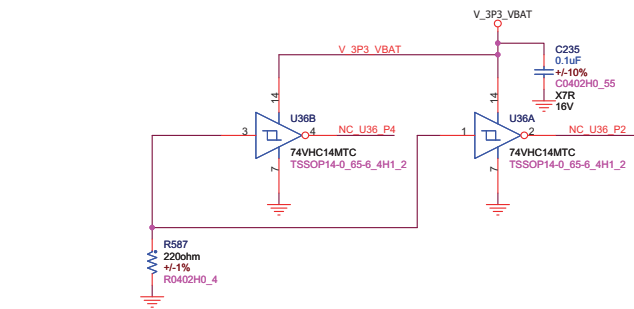
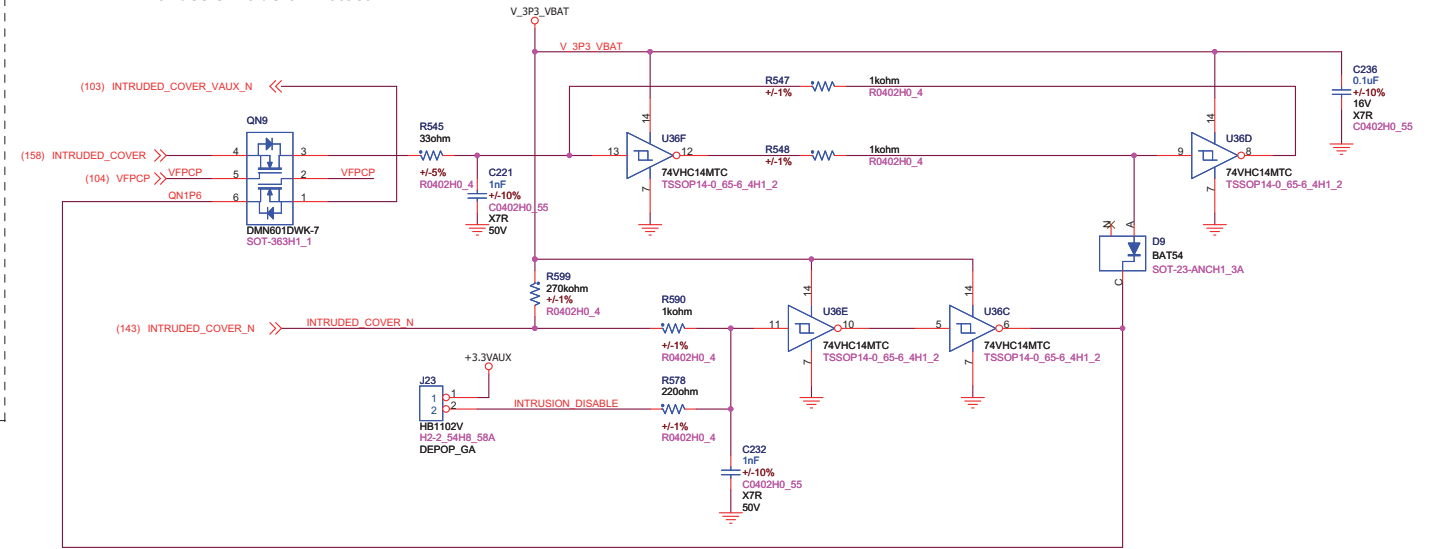
NOTE: Planar rev is not equivalent to PWB rev
Planar rev is meant to show boards that are different from a configuration/feature point of view



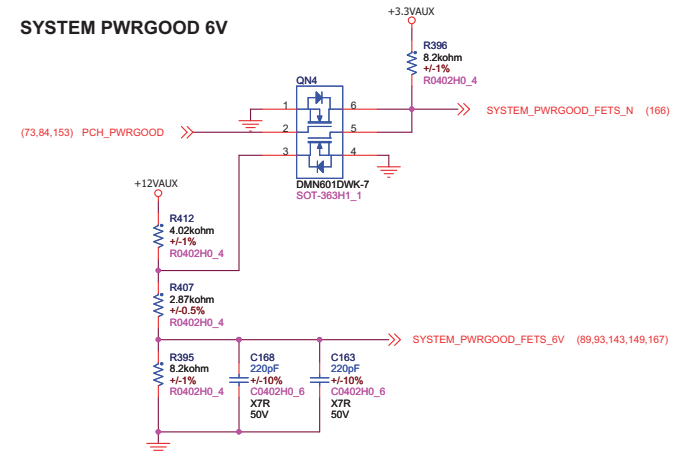
VFPCP



<http://adf.ly/3o8pJ>
Chassis Intrusion Detect

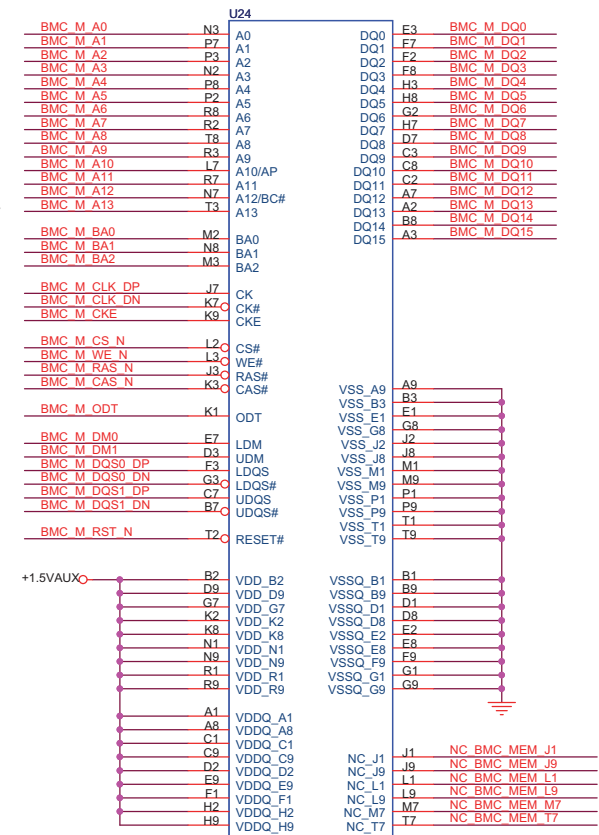
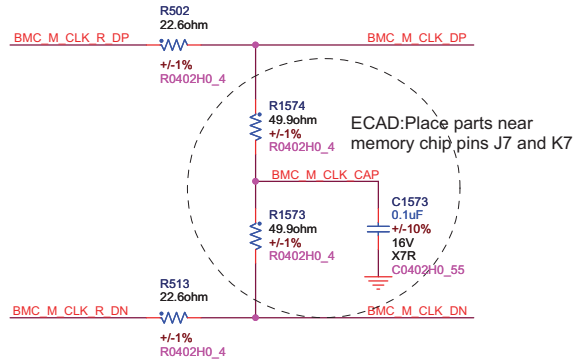
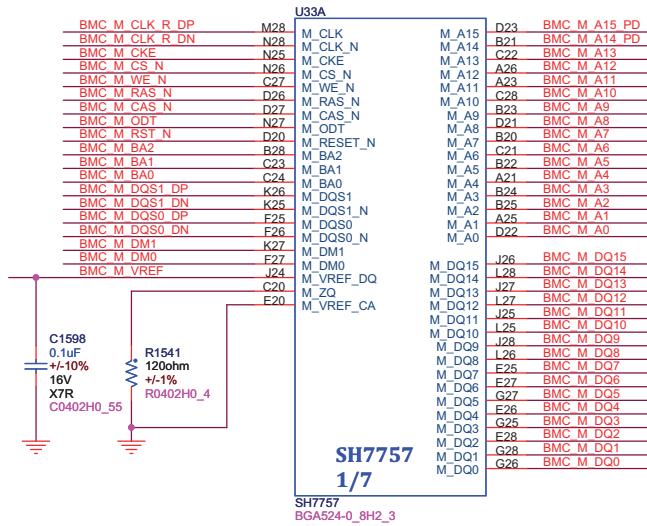


SYSTEM PWRGOOD 6V

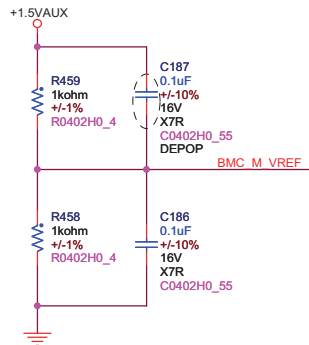


Need to be applied

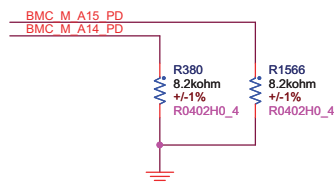
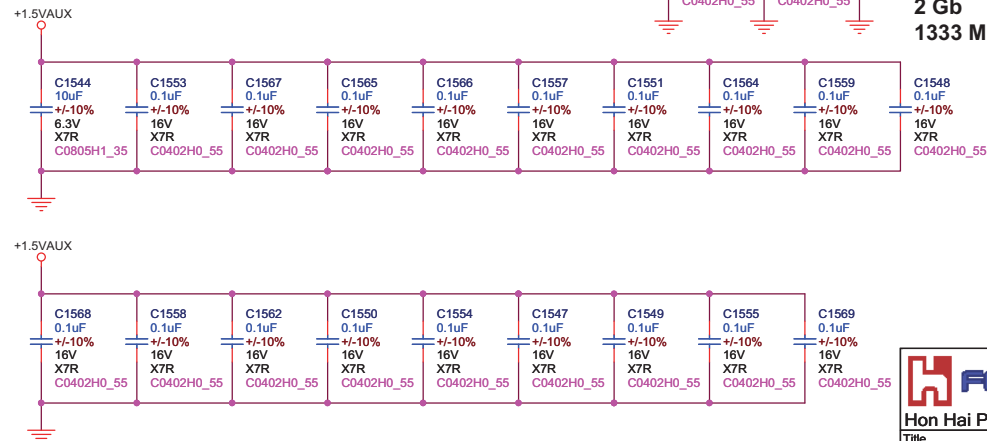
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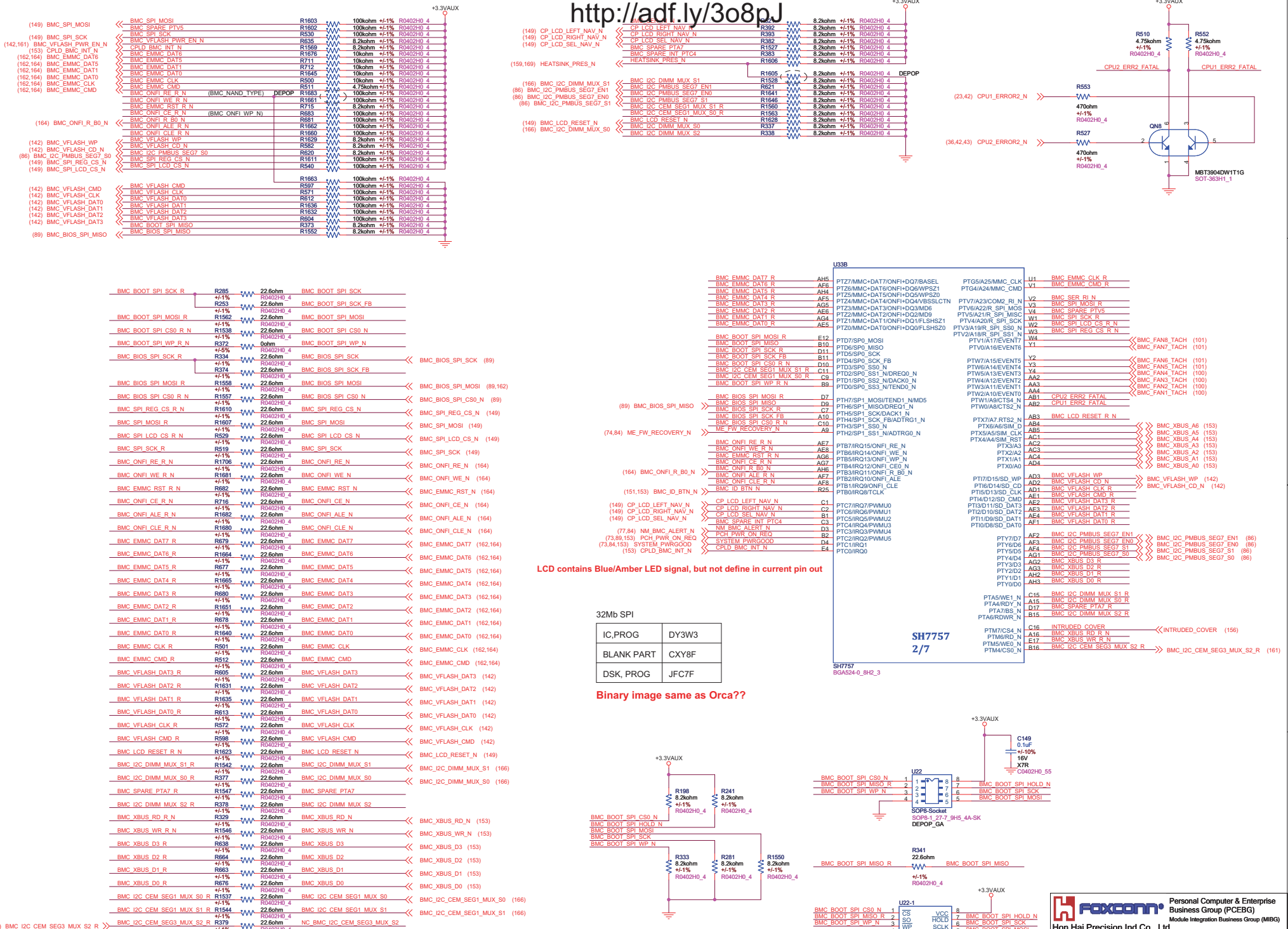
ECAD:Place in between iDRAC BGA and memory area



ECAD:Place near DRAM

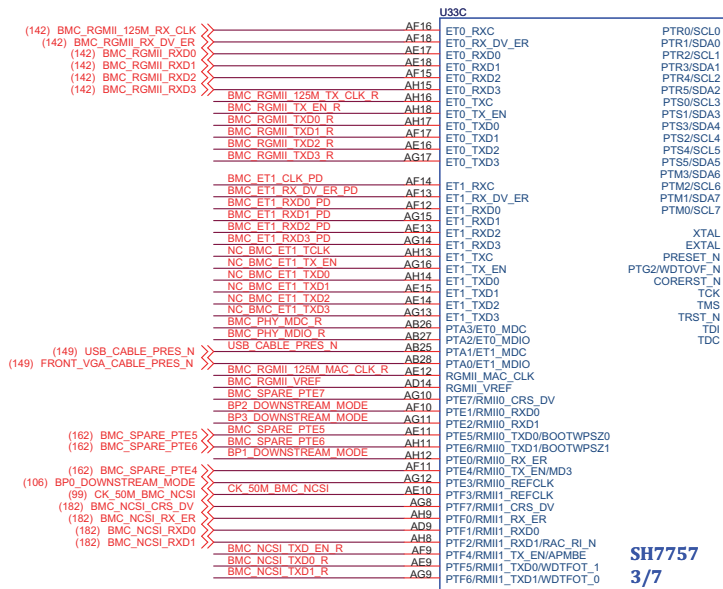


<http://adf.ly/3o8pJ>



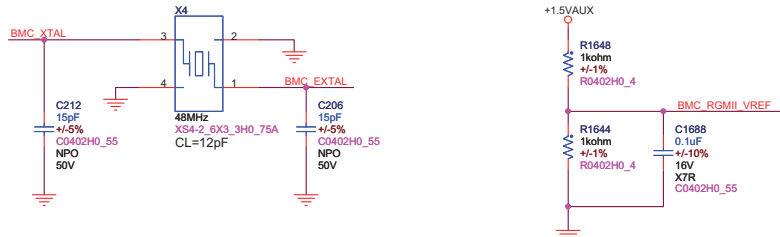
http://adf.ly/3o8pJ

Remove U31.AE15 NC net for BMC_RGMII_VREF trace width.

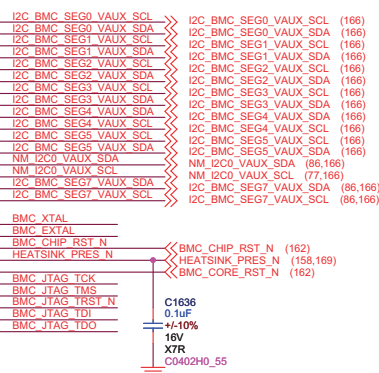
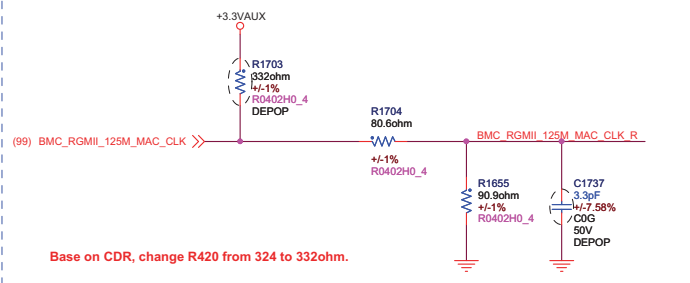


BMC_NCSI_RX_ER don't connect to NDC

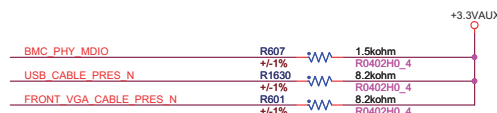
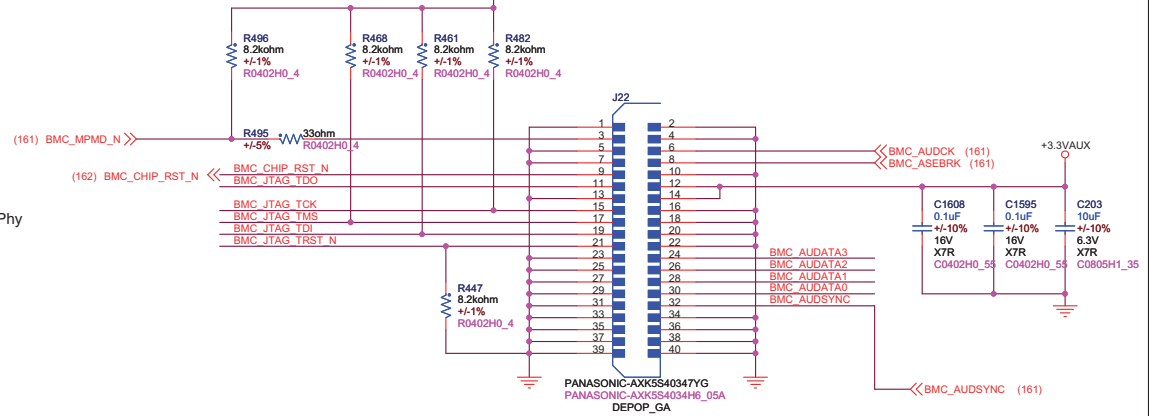
Ball AB25, AB28, AG10, AF10, AG11, AH11, AH12, AF11, AG12 are for blade 10/100 Phy
Ball AB28, use as RGMII clock enable for monolithic



ECAD: place these 3 resistors near U_CKMNNG_Plus

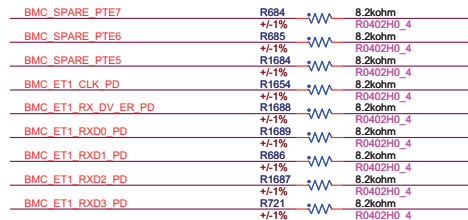
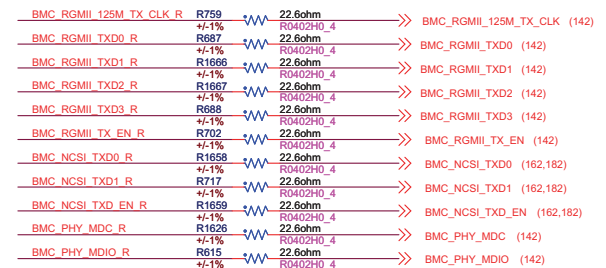


ECAD: Close to PCH Heatsink



NOTE: These are not PWM outputs when the PJET is running.

ECAD: Place close to iDRAC.



SDS don't have BP1/BP2/BP3

FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)

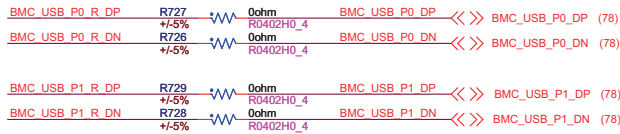
Hon Hai Precision Ind.Co., Ltd.

Title: iDRAC7 I2C/ETH/JTAG/CLK

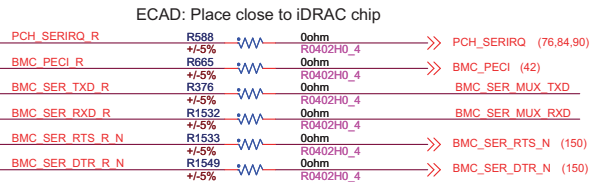
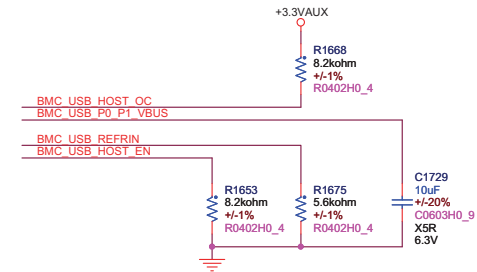
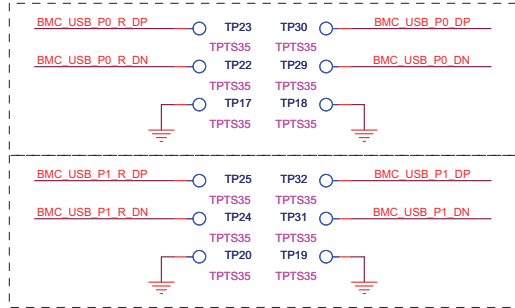
Document Number: 01015C800-000-G
PCB P/N: 01292011, 10:57 AM

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Rev X00

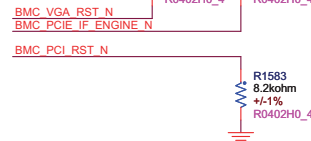
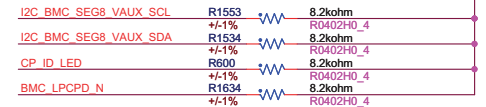
ECAD:Place on topside in accessible area.



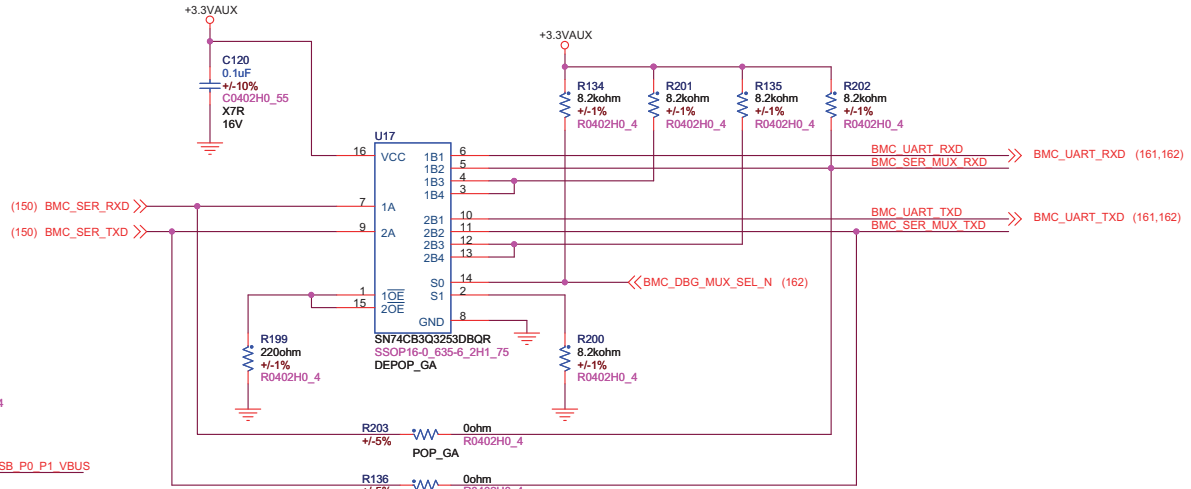
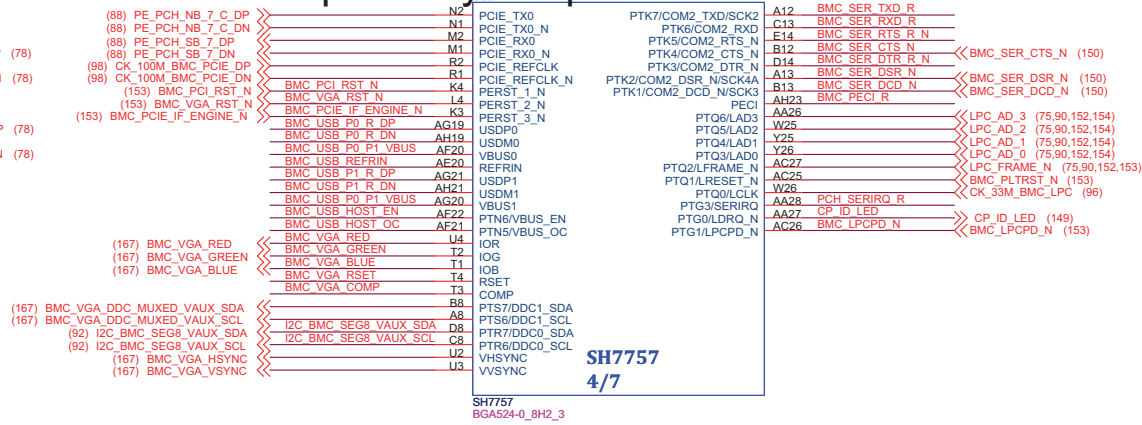
ECAD:Place GND TP near respective USB TP's.



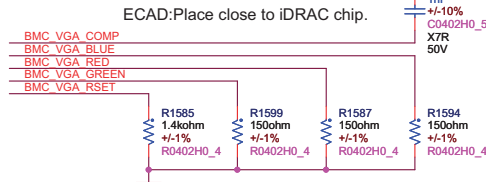
seg8 goes to backplane and isolation to main is on the backplane



<http://adf.ly/3o8pJ>

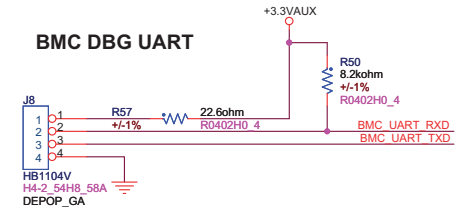


ECAD:Place close to U55



Monolithic: Use BMC_VGA_RSET 1.4K for driving 37.5Ohm to 700mV full white
Blade: Use BMC_VGA_RSET 1.5K for driving 250hm to 435mV full white

BMC DBG UART

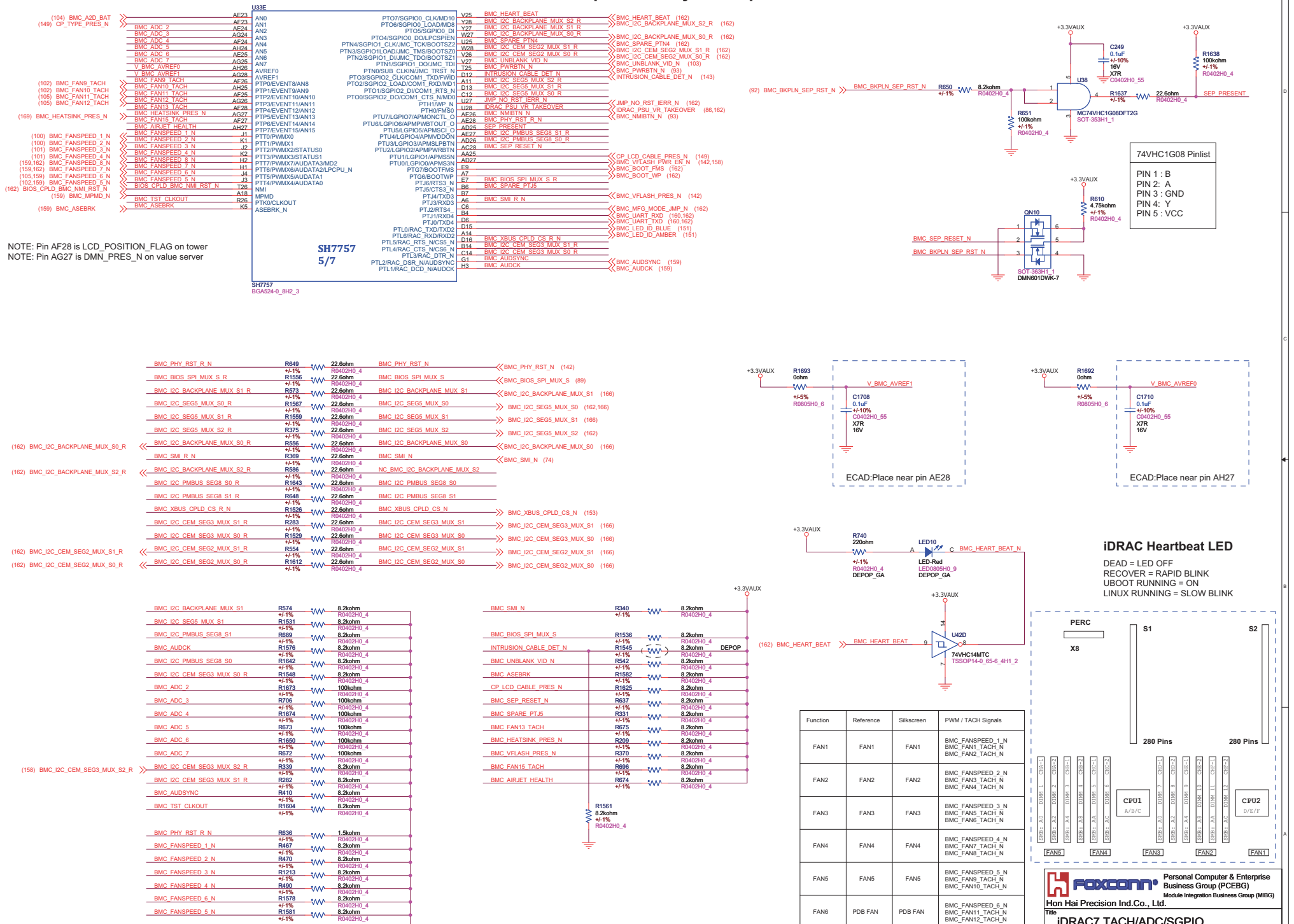


FOXCONN Personal Computer & Enterprise Business Group (PCEBG)
Module Integration Business Group (MIBG)
Hon Hai Precision Ind. Co., Ltd.

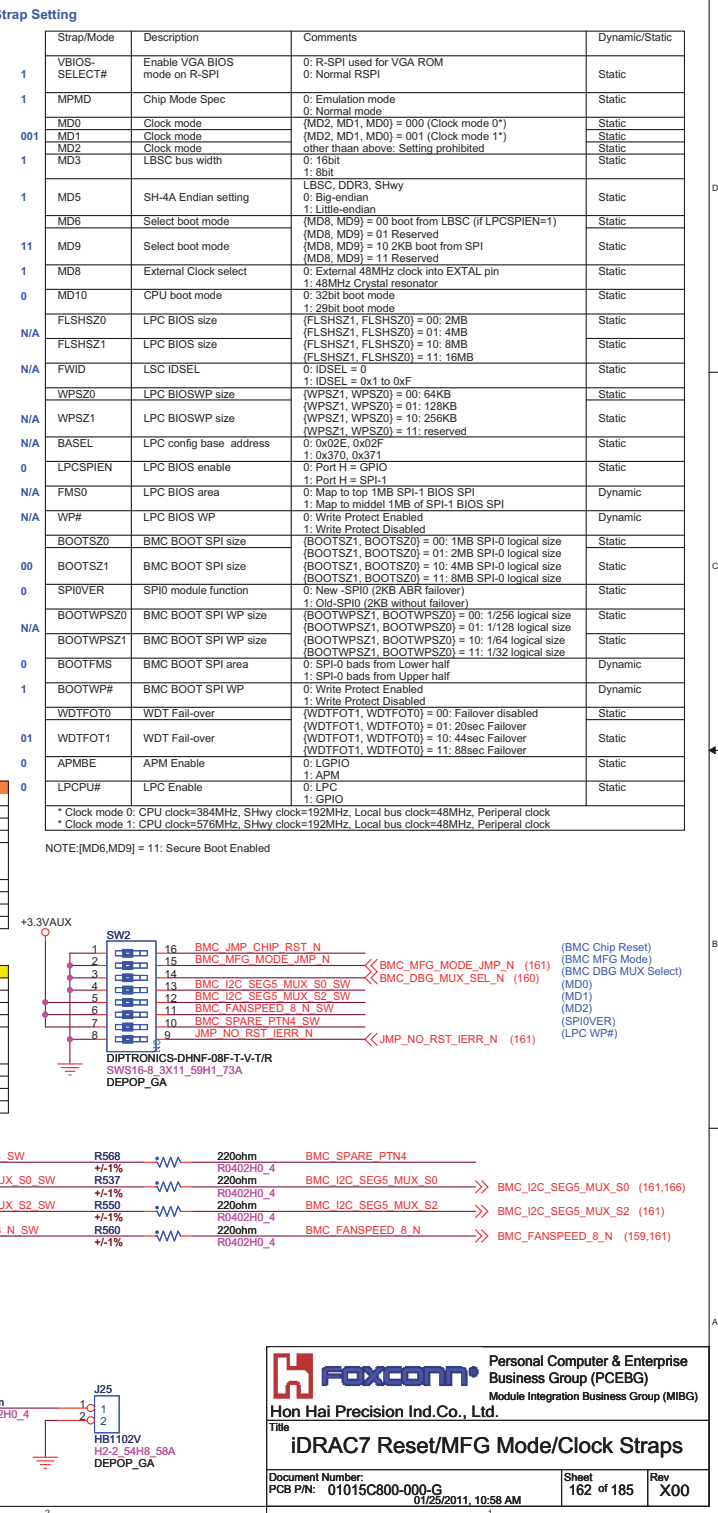
iDRAC7 USB/PCIE/VGA/COM/LPC

Document Number: 01015C800-000-G
PCB P/N: 01015C800-000-G
01/25/2011, 10:57 AM

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Rev X00

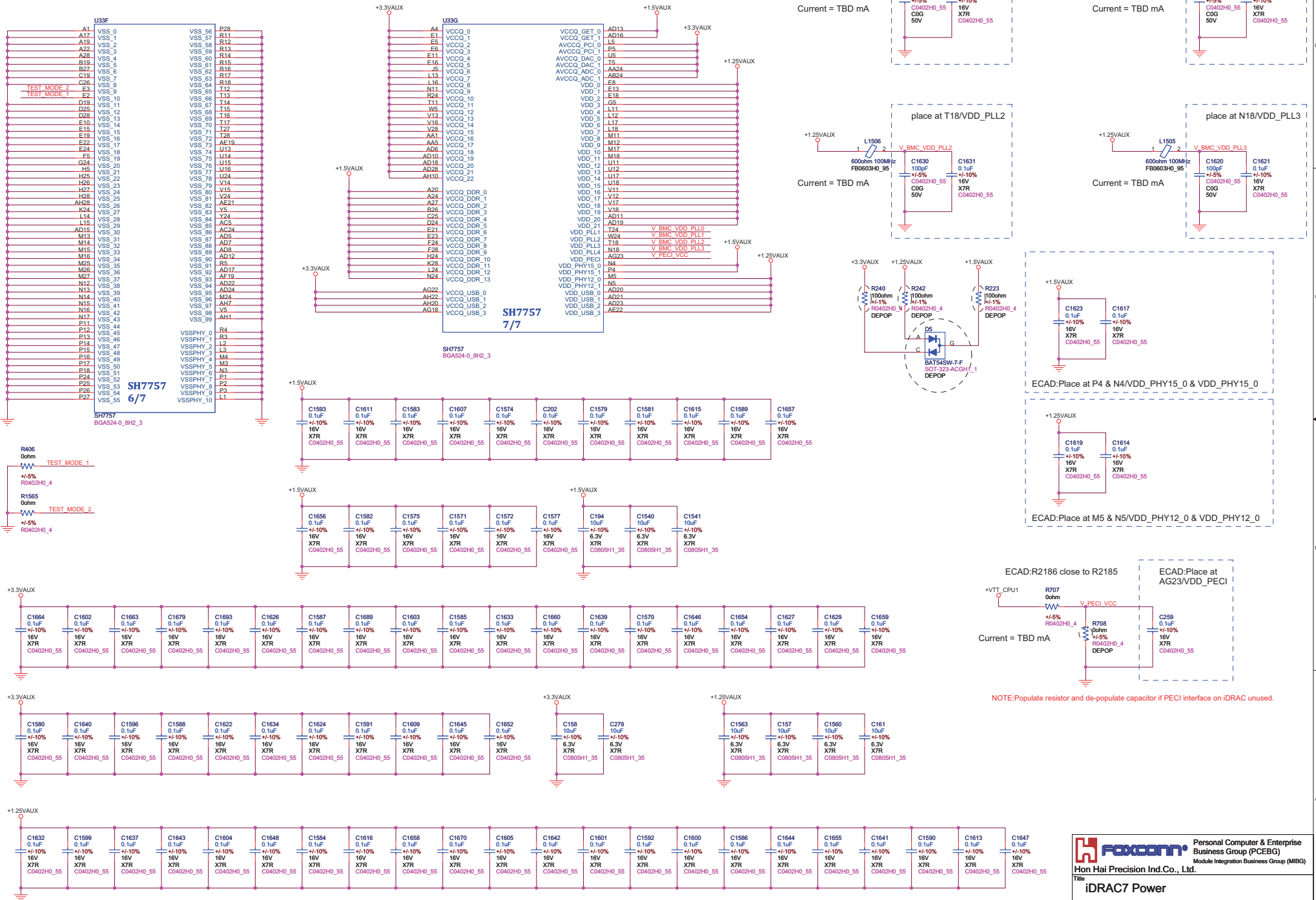


iDRAC Strap Setting



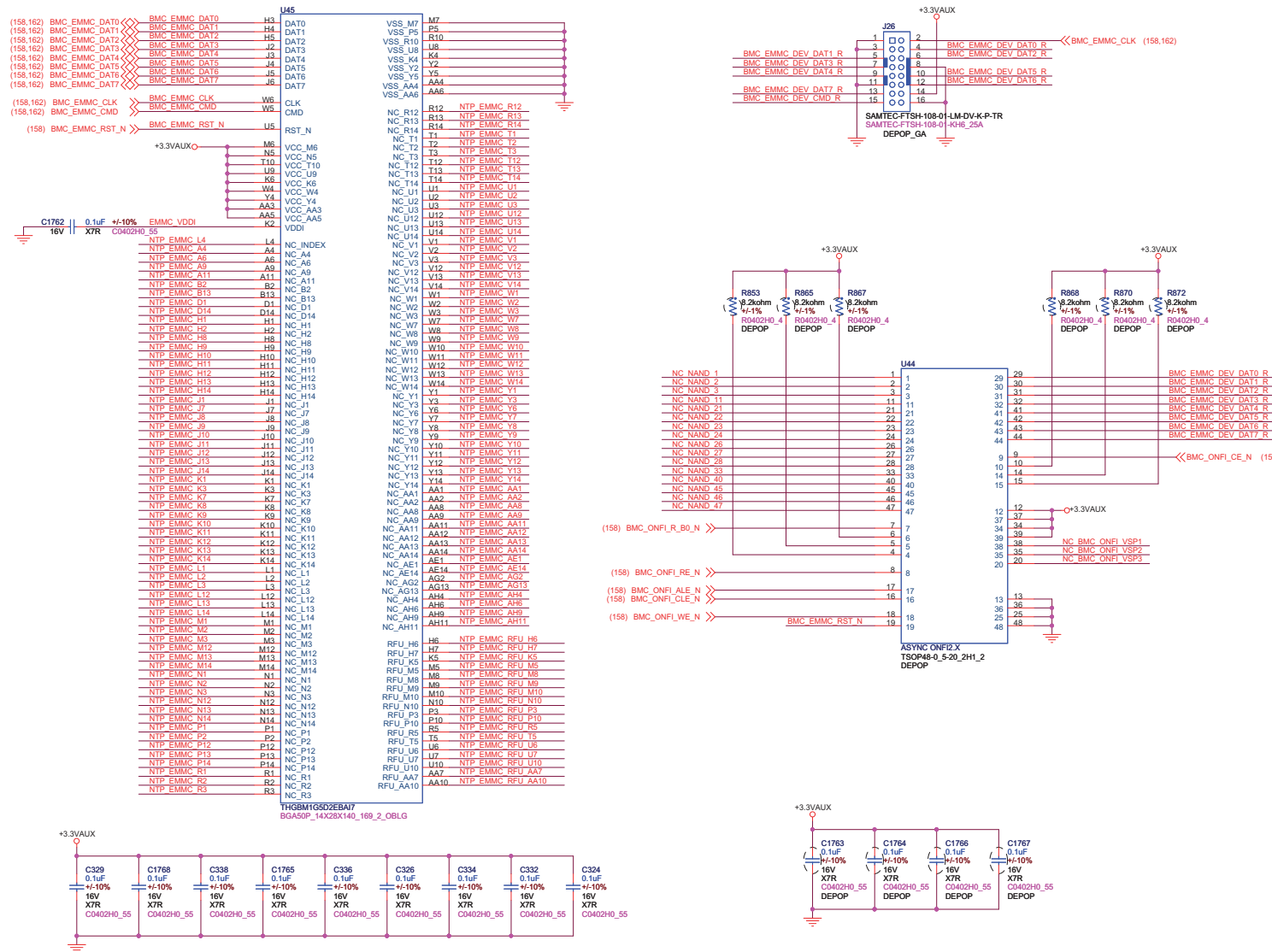
ECAD: Place on top side.

<http://adf.ly/3o8pJ>



NOTE:Some pads are oblong NSMD to allow for direct attach 4/4 routing.

<http://adf.ly/3o8pJ>



IC, PROG	987M3
BLANK PART	CVRYX
DSK, PROG	CG5X1

ECAD: Place series resistors near U69 (Interposer)

